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Analysis of Single Phase Diode Clamped Three Level Inverter

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Abstract: The elementary concept of a multilevel converter is to achieve high power by using a series of a power semiconductor switches with lower voltage D.C source. The output voltage waveform of a multi-level inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. In this paper, single phase diode clamp multilevel inverter topology is analyzed by employing SPWM technique which controls the switching operation. Circuit configuration and theoretical operation are also discussed. The performance of the topology is investigated through MATLAB based simulation results.

Keywords: *Diode Clamp Multilevel Inverter, Sinusoidal PWM Technique, Total Harmonic Distortion.*

I. INTRODUCTION

Multilevel inverter is a power electronics device which is capable of providing desired alternating voltage level at the output using multiple lower level D.C voltage as an input. Mostly a two level inverter is used in order to generate the A.C voltage from D.C voltage. Now the questions arises what is the need of using multilevel inverter when we have two-level inverter.

First we need to look at the concept of multilevel inverter. First take the case of a two level inverter. A two level inverter creates two different voltage for the load i.e suppose we are providing Vdc as an input to a two level inverter then it will provide +Vdc/2 and –Vdc/2 on output.To build up an AC output voltage these two voltages are usually switched with PWM.Though this method is effective it creates harmonic distortions in the output voltage, EMI and high dv/dt (compared to multilevel inverters). This may not always be a problem but for some applications there may be a need for low distortion in the output voltage. The concept of Multilevel Inverters (MLI) does not depend on just two levels of voltage to create an AC signal. Instead several voltage levels are added to each other to create a smoother stepped waveform with lower dv/dt and lower harmonic distortions.With more voltage levels in the inverter the waveform it creates becomes smoother, but with many levels the design become with more components and a more complicated controller for the inverter is needed.

DIODE CLAMP MULTILEVEL INVERTER TOPOLOGY:-

In this topology there are two pairs of switches and two diodes are consists in a three-level diode clamped inverter. All switch pairsworks in complimentary mode and the diodes used to provide access to mid-point voltage. The DC bus voltage is dividing into three voltage levels with the help of two series connections of DC capacitors, C1 and C2. With the help of the clamping diodes Dc1 and Dc2 the voltage stress across each switching device is partial to Vdc. It is supposed that the total dc link voltage is Vdc and mid-point is synchronized at half of the dc link voltage, the voltage across each capacitor is Vdc/2 (Vc1=Vc2=Vdc/2). In a three level diode clamped inverter there are three different feasible switching states which apply the stair case voltage on outputvoltage relating to DC link capacitor voltage rate. At any time a set of two switches is on for a three-level inverter and so on.

II. WORKING

Figure1 shows a three level diode clamp converter in which the dc bus consists of two capacitors C1 and C2. For dc-bus voltage E, the voltage across each capacitor is E/2 and each device voltage stress will be limited to one capacitor voltage level E/2 through clamping diodes.

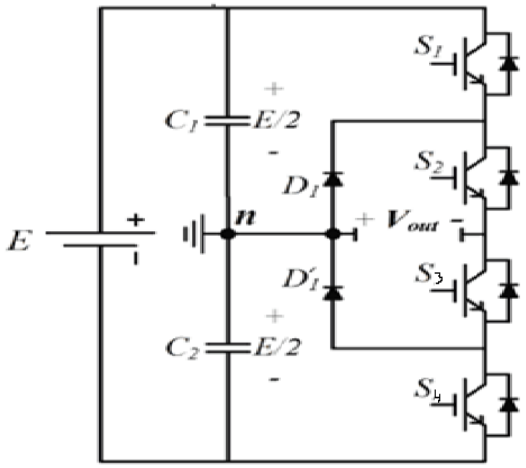

Figure 1: Circuit Diagram of three level inverter

Table1: Switching State Of The Three Level Diode Clamp Inverter.

Switching status	State	voltages
S1= ON, S2= ON	+ve voltage	Vao=Vdc/2
S2=ON,S3=ON	0	Vao=0
S3=ON,S4=ON	-ve voltage	Vao=-Vdc/2

To explicate how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. Above table 1 shows that S1 and S3 are complementary each other. And similarly S2 and S4 are complementary each other.

III. CONTROL TECHNIQUES

The sinusoidal PWM technique is very popular for industrial converters. In this technique, an isosceles triangle carrier wave of frequency fc is compared with the fundamental frequency f sinusoidal modulating wave and the points of intersection determines the switching points of power devices.

Three level pulse width modulated waveforms can be generated by sine-carrier PWM. Sine-carrier PWM is generated by comparing the three reference control signals with two triangular carrier waves.

IV. SIMULATION RESULT

Simulation of Single phase diode clamped inverter using sinusoidal pulse widthmodulation was carried out with the help of "MATLAB R2013a". Simulation wascarried out to observe the improvement in the line voltage THD in 3-Level inverter.

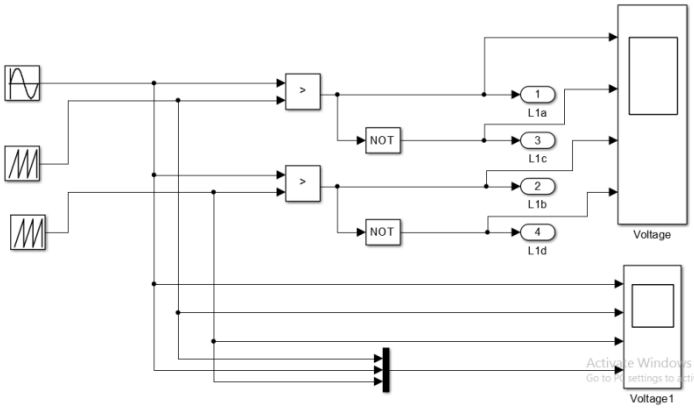

Figure 2: Circuit Diagram of PWM generation

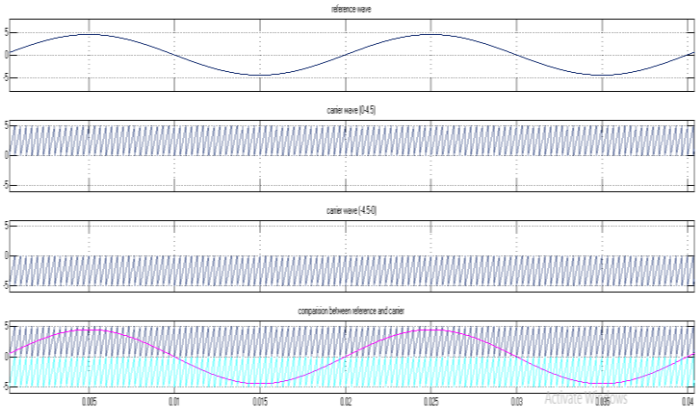

Figure 3: Reference and carrier waveform comparison

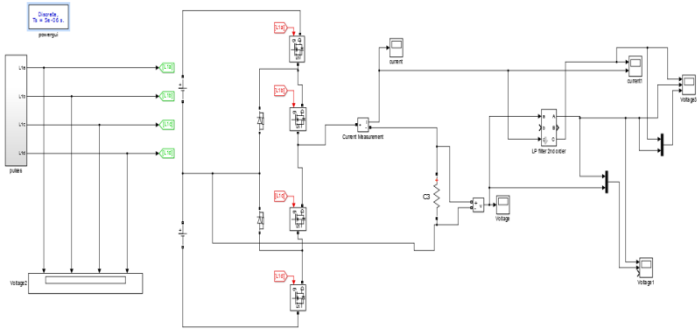

Figure 4: Circuit of Diode Clamp three level Inverter

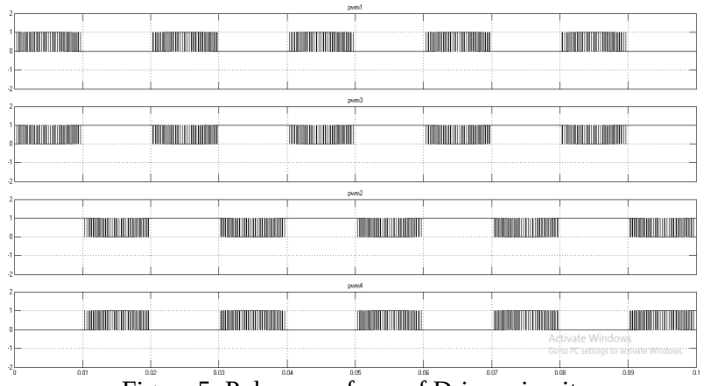

Figure 5: Pulse waveform of Driver circuit

Specification for three level Inverter:-

Supply Voltage =324V
Fundamental Frequency(f_r)=50Hz
Switching Frequency(f_s) =3000Hz
Amplitude Modulation Index(m_a)=0.9

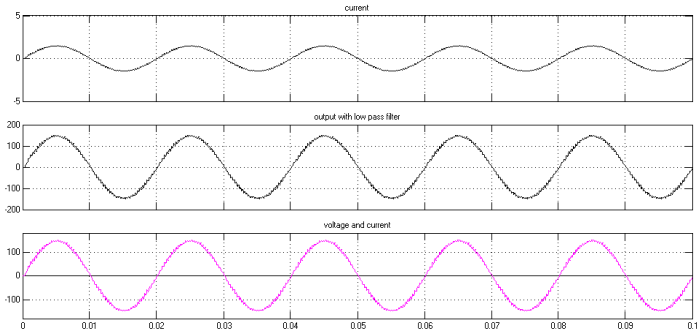

Figure 6: Waveform with lowpass filter

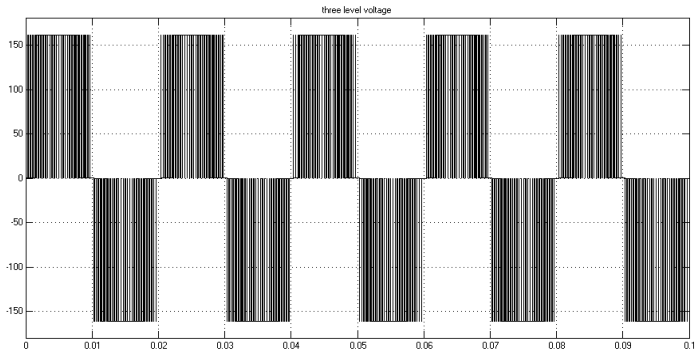

Figure 7: Output waveform of Three level inverter

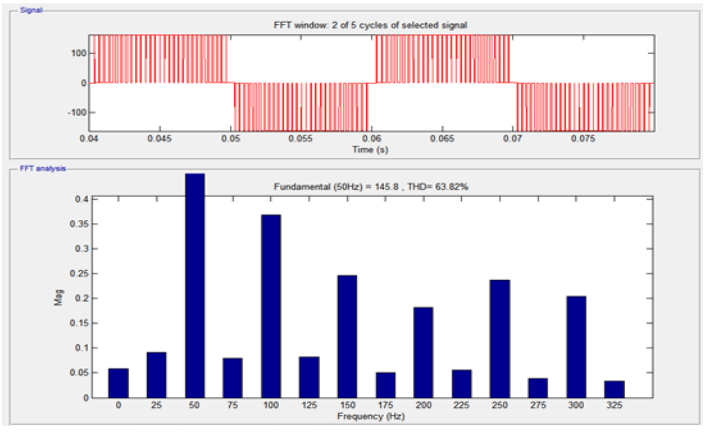

Figure 8: FFT Analysis without filter

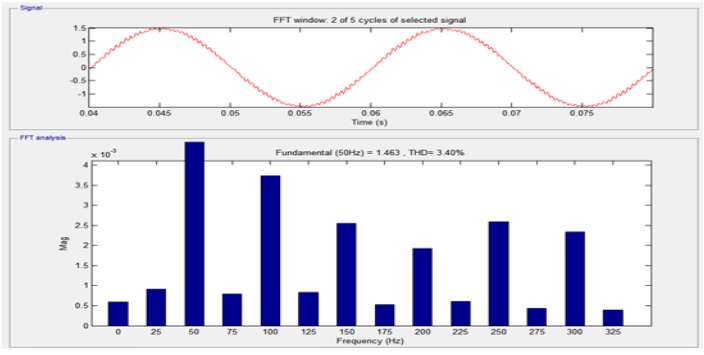

Figure 9: FFT Analysis with filter

Result without filter:-

Frequency	*Load*	*THD*
fundamental	R-100ohm	63.82%

Result with Filter:-
Filter- Cut off Frequency=750Hz
Damping Factor=0.307

Frequency	*Load*	*THD*
Fundamental	R- 100ohm	3.40%

CONCLUSION

The simulation of 3-Level Diode clamped multilevel inverter was carried using sinusoidal pulse width modulation (PWM). It has shown that reduction in line voltage THD takes place in three level inverter and performance of these inverters were investigated using R Load.

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