

Comparative Analysis of High Speed FBB TSPC and E-TSPC Frequency Divider at 32 nm CMOS process

¹Abhishek Agrawal and ²Nikhil Saxena,

¹PG Scholar, ²Assistant Professor,

^{1,2}Department of Electronics and Communication, Institute of Technology and Management, Gwalior, India

Abstract: In this current paper execution of forward body biased True Single Phase Clock (FBBTSPC) and forward body biased extended True Single Phase Clock (FBBETSPC) are investigated. The delay of FBBTSPC and FBBETSPC are analyzed, simulated, executed and compared with the existing TSPC and ETSPC. A high speed divide-by-2 unit of frequency divider divide by two with the body biased is proposed and validated that this frequency divider divide by two can operate with higher frequency of 4 GHz stably on a 180 nm technology. This frequency divider divide by two with the body bias design can be widely used in Communication data analysis probe systems.

Keywords: CMOS integrated circuit, D flip-flop (DFF), frequency divider, frequency synthesizer, high-speed digital circuit, true single-phase clock (TSPC), Extended true single-phase clock (E-TSPC), HSPICE

I. INTRODUCTION

As transistor size scaling of the feature size in the CMOS devices continues, the lower downs, requires the reduction of power consumption on electronics devices, especially on power aware VLSI such as implantable bio-medical equipments and portable hand held devices such as mobile phones, has become one of the fashionable design concerns in today's radio frequency integrated chips (RFICs). To reduce or lower down the power dissipation of computers, ultra-low-voltage functional operation has become one possible important solution, especially for digital circuits where supply voltage has been continuously reduced below the threshold voltage. However, it is hard to reduce ultra low voltage functioning together with analog and RF circuits since the system performances would decrease significantly, under the obstacles of signal amplitude. The TSPC[1] and E-TSPC[2] architecture technique based frequency divider divide by two is a synchronous circuit which is implemented using by D flip-flops and additional logic gates. Due to the incorporation of additional logic gates between the flip-flops to achieve the two different division ratios, the speed of the frequency divider divide by two is affected and the switching power increases. Various flip-flops have been proposed to improve the operating speed of dual-modulus frequency divider divide by twos. The optimization of the D flip-flop in the synchronous stage is essential to increase the operating frequency and reduce the power consumption. The high speed operation of MOS transistors is limited by their low transconductance. Therefore, dynamic and sequential circuit techniques or clocked logic gates such as, true single phase clock (TSPC) and Extended true single phase clocking (ETSPC) must be used in designing synchronous circuits to reduce circuit complexity, increase operating speed, and reduce power dissipation.. The dual-modulus frequency divider divide by two could also be used in the feedback to obtain fractional output frequencies. The power consumption and frequency of operation of TSPC and E-TSPC 2 frequency divider divide by twos are to be analyzed and an ultra-low power TSPC 2 frequency divider divide by two is designed. Based on this design a 32/33 or higher

order frequency divider divide by two can be implemented, which is highly suitable for high resolution fully programmable[3] frequency synthesizers.

II. TSPC AND E-TSPC D FLIP FLOP

In this present paper the low power consumption and operating frequency of true single phase clock (TSPC) and extended true single phase clock (E-TSPC) frequency divider divide by two are executed which are designed by using TSPC and E-TSPC frequency dividers as shown in figure 1 and figure 2 which is then analyzed and modeled. Based on this research a new low power and improved operating speed TSPC divide by 2 frequency divider is proposed which is silicon verified. In Comparison with the existing TSPC and E-TSPC architectures the proposed divide by 2 frequency divider divide by two or frequency divider is capable of operating up to 10 GHz with 32nm CMOS methodology and ideally, a considerable reduction in power consumption is achieved when compared under the same technology at supply voltage of 1 V This extremely low power Consumption which is achieved by radically minimizing the sizes of MOSFET[4] transistors, reducing the number of switching stages or levels and blocking the power supply to one of the D flip-flops (DFF) during Divide-by-2 operation. In this work the short-circuit power and the switching power in the TSPC and E-TSPC -based divider are calculated and simulated and there comparisons are illustrated.

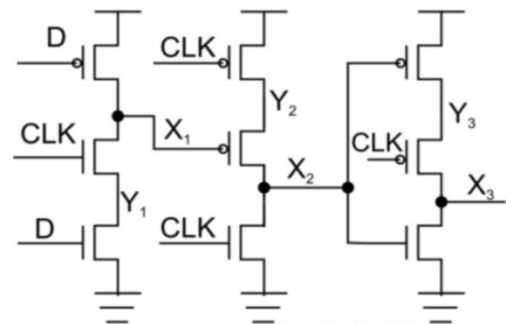


Figure 1: TSPC architecture based D flip flop.

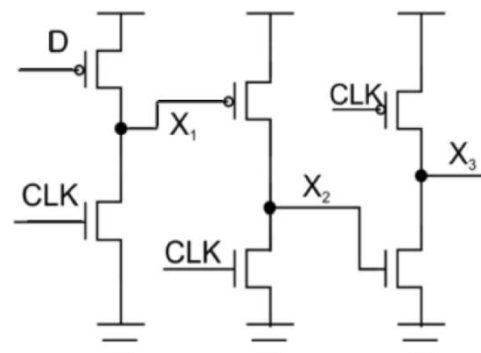


Figure 2 E-TSPC architecture based D Flip-flop.

III. TSPC ARCHITECTURE BASED FREQUENCY DIVIDER DIVIDES BY 2

In this particular circuit there are 9 MOSFET and two extra for inverter it means total 11 transistors are used whose channel length is 32nm, i.e. in this paper work is being done on 32 nm technology. 2 additional MOSFET transistors are used as NOT Gate i.e. total 11 transistors are used in TSPC D flip flop, which is further feed backed and divide by 2 frequency divider is realized and simulated using HSPICE simulator. Clk(in) is input node from which input frequency of desired frequency is given to the circuit, this circuit is operated on positive edge of clock pulse and at output node clk(out) divided frequency by half is obtained. This circuit can be widely used in clock distribution within circuit which requires different frequency other than input frequency, higher order frequency dividers can also be realized by using this divide by frequency divider. By changing gate width Divide-by-3 frequency divider can also be realized. A low-power divide-by-2 unit of a frequency divider divide by two is proposed and implemented using a CMOS technology. Compared with the existing design, reduction of power consumption is demonstrated.

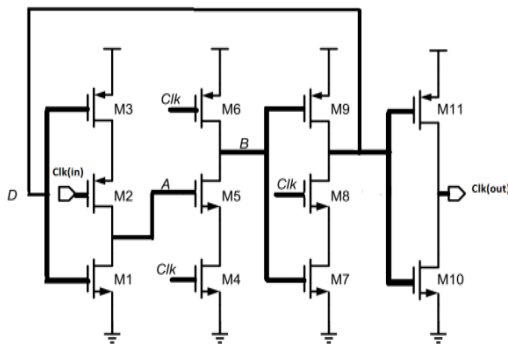


Figure 3: TSPC Based Divide by -2 CMOS frequency divider.

B.E-TSPC based divide by 2 frequency divider

E-TSPC logic based frequency divider is realized by using 3 levels of 2 transistors i.e. it comprise of total 6 transistors further its output node of E-TSPC logic based d flip flop is feed backed to realize divide-by-2 frequency divider divide by two which is suitable for low supply voltage and low power applications have been designed and implemented wherein the counting logic and the mode selection control[5] are implemented using a single transistor. Thus the critical path is reduced which in turn enhances or increases its working or operating frequency. Compared with the conventional TSPC and E-TSPC based 2/3 frequency divider divide by two designs as much as PDP, operation speed and reduction in area can be achieved by the proposed design. In this paper True Single Phase Clock (TSPC) based on Ratio logic D flip-flop is implemented in 32nm CMOS process. A Glitch elimination TSPC D-flip flop is used in the synchronous counter. The power efficient TSPC design technique is applied to division by 2, and their performances are compared. Simulation and measurement results have been shown as high-speed, low-power, low power delay product (PDP) and multiple division ratio capabilities of the power efficient technique with a frequency range of 0.5-10GHz[6]. The improved speed, the power efficiency, and the flexibility will promote its wide deployment in Multi gigahertz range applications.

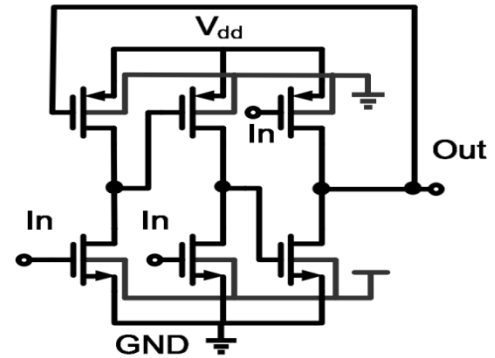


Figure 4 E-TSPC Based Divide by -2 CMOS frequency divider.

IV. CIRCUIT DESIGN ISSUES AND PERFORMANCES

As shown in figure 2 and figure 4 E-TSPC flip-flop uses only two transistors in each level while a TSPC flip-flop uses three transistors of various dynamic logic CMOS circuit techniques, TSPC architecture based CMOS circuit is operated with one single clock signal only to avoid clock skew problems. Frequency divider circuit is implemented using forward body biasing technique(FBB)[2] A True Single Phase Clock (TSPC) flip-flop configured to operate in an present state and hold mode, comprising as integral parts: an input stage having an input node and a first output node, a middle stage or second stage having a second output node, an output or third stage having a third output node which is feedback to first state input node to construct frequency divider, and a reset functional block can be switchable between an activated and deactivated mode of the circuit operation. The reset functional stage of TSPC frequency divider circuit resets the D flip-flop when activated and is configured to synchronous exit out of reset when switched from its activated to deactivated mode of operation so that an output signal of the flip-flop is only up-dated when the D flip-flop transits to its next state mode. TSPC flip-flops are clocked by a single clock signal which alternates between a first state associated with the present state mode and a second state associated with the hold mode. Substantially, the output signal of a TSPC frequency divider of the inventive flip-flop is present at the third node if necessary, the signal at the third node may be inverted by an inverter in this paper the frequency divider circuit implemented using TSPC technique is inverted by adding inverter at the output node. The output signal of the circuit interconnects of the inventive frequency divider can have two states, namely logical value "1", more often it is associated with a high voltage and logical "0", usually associated with a low voltage i.e. 0 V . When the circuit frequency divider of the inventive flip-flop is in reset mode, then the output signal is set to logical "0". Since the reset function is a synchronous exit out of reset function i.e. applied clock frequency, the output value of the flip-flop must only be up-dated with the positive edge of the clock signal transits from its hold mode to its evaluating mode when the reset is turned deactivate. In the proposed method the body pin of the transistor is connected to source and some positive voltage is applied with respect to source. In the body biasing technique the drain current is decreases and threshold voltage is increases this is due to body effect of MOSFET device. Hence the total power consumption is decrease as compared to traditional techniques.

V. SIMULATION RESULTS

All simulation results have been carried out by using the HSpice program simulator based on 32 nm CMOS technology, level

54.shows all nodes signal of the proposed divide-by-2 circuit with 1.2 volt supply voltage a 1GHz when the MC input is in LOW state. Fig. Shows al nodes signal of the proposed divide-by-2 circuit with 1 volt supply voltage at 10 GHz when the clock input is in HIGH state. In this work parameters like leakage current, leakage power with grounded input node is estimated, propagation delay and total power dissipation is estimated and arranged in table 1 and compared results are shown on the table with E-TSPC based frequency divider. Without applying FBB technique, at the power supply of 0.5-V, the divide-by-2 circuit fails to response according to simulation results. As the power supply increasing to 0.7-V, the divide-by-2 circuit starts to work and the maximum operation frequency is 4GHz. By applying FBB technique, at the power of 0.5-V, measurement results show that the divide-by-2 circuit works properly and the maximum operation frequency is 7.2GHz, which could meet the requirement of divider stage 1. The measured input sensitivity of divider stage 1 in divide-by-2 operation According to the literature survey, it is the first time to implement high frequency divider under the power supply of 0.5-V.

Table 1: TSPC and E-TSPC frequency divider parameter comparison.

Parameters	TSPC	TSPC	E-TSPC	E-TSPC
Technology	180	32 nm	180	32 nm
Delay	-	5.2489 ns	-	0.46406 ns
Leakage Power	-	13.9363 pW	-	16.8784 nW
Leakage current	-	19.9090 pA	-	33.7569 nA
Power dissipation	0.7 mW	886.6856 pW	240 μW	47.4688 nW
Applied node voltage	1V	0.7V	0.9	0.5V
Temperature	-	25°C	-	25°C
Year	2012	-	2015	-

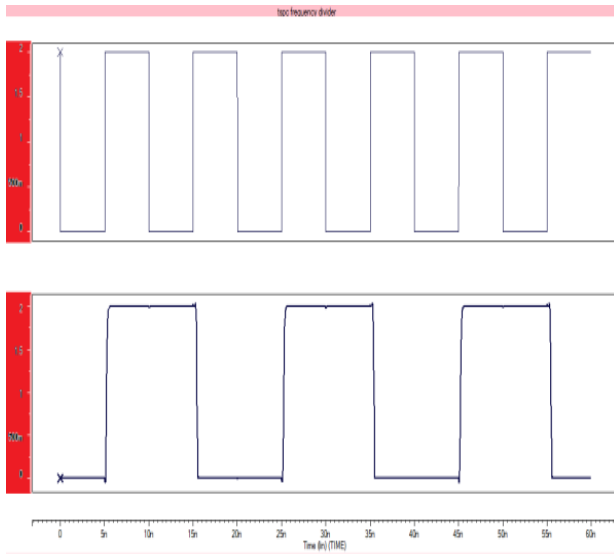


Figure 5: TSPC Based frequency divider input and output waveform divide by 2 operation

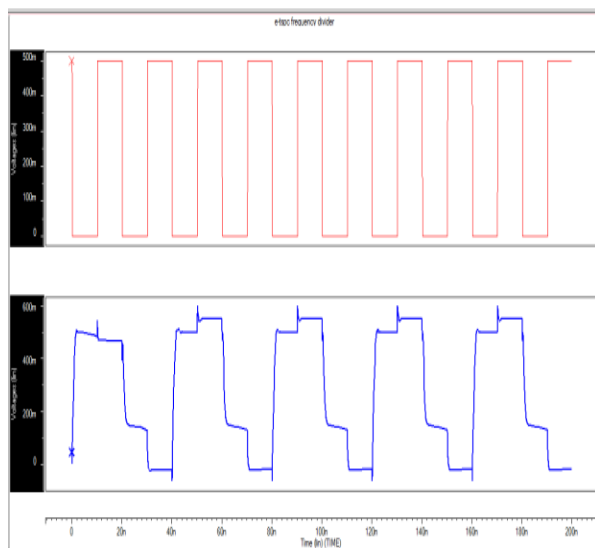


Figure 6: E-TSPC Based frequency divider input and output waveform divide by 2 operation.

A. Analysis of TSPC and E-TSPC Frequency divider on varying voltage

1. Leakage Power

Leakage power is the result of unwanted unnecessary sub-threshold current in the MOSFET transistor channel when the device is turned off. This sub-threshold-driven leakage power is strongly influenced[7] or effected by variations in the transistor threshold voltage V_T (V_t voltage applied to the gate electrode that turns on the transistor When power is dissipated or consumed by the device, it invariably leads to rise in temperature of the chip which causes dissipate more power by the circuit. This rise in temperature affects the device both when the device is off as well as when the device is on. Total Power dissipation is the sum of static and dynamic Power dissipation. Static power is also known as leakage power. Figure 7 shows the comparative plot of Leakage power of TSPC and E-TSPC architecture based frequency divider on different node voltages, it is observed that exponential growth[8] in MOSFET device power consumption as rise in every 0.1 V node voltage. The simulation is done from 0.7 V to 1.5 volts, as Forward Body Bias technique is used so this circuit can be operate beyond threshold level i.e. 0.5V

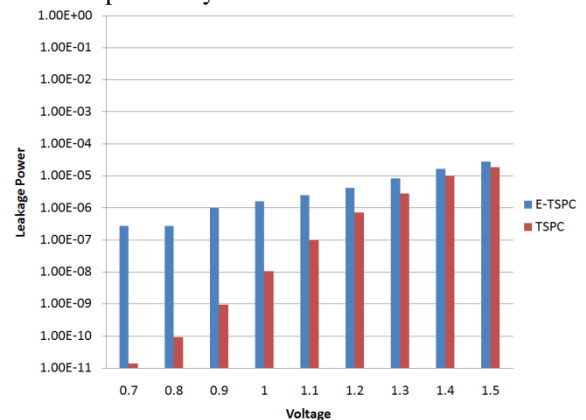


Figure 7: Voltage versus Leakage power Comparison plot of TSPC and E-TSPC architecture based frequency divider.

2. Leakage Current

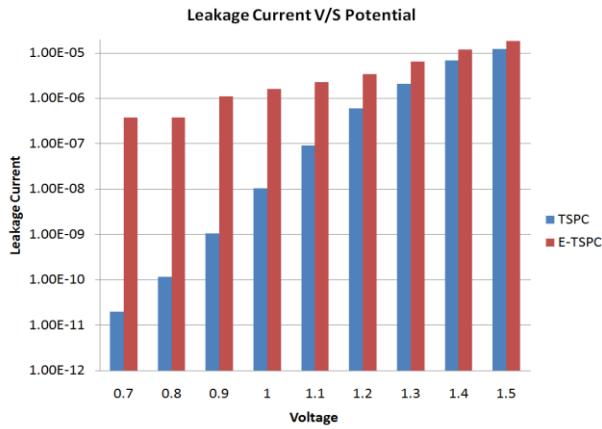


Figure 8: Leakage current v/s Potential of TSPC and E-TSPC Frequency dividers.

Figure 8 shows the comparison of leakage current between TSPC and E-TSPC frequency divider circuits, the simulated results are compared for the parameter leakage current E-TSPC architecture based frequency divider circuit has more leakage current drawn[9] as compared to TSPC frequency divider, but in terms of operational speed and chip area E-TSPC has advantage over TSPC architecture based circuit. Leakage current is the current drawn by the circuit when it is in standby mode or in ideal mode, i.e. it not used by distributed system inside mainframe processors.

3. Power dissipation

The power dissipation of a circuit is define as the total DC power consumed by the digital circuit by its applied dc power source that is drain voltage which is applied on the drain terminal[10] of the MOSFETS in the circuit. Figure 9 shows a plot of power dissipation versus potential of TSPC and E-TSPC frequency dividers, there are total 11 and 6 MOSFET devices respectively are used to construct typical TSPC and E-TSPC frequency divider Cell which divides input frequency in half as its output. Figure 6 shows the variation of power dissipation with respect to applied voltage, as the voltage increases power consumed by the circuit is increased. To optimize the power dissipation further power optimization techniques can be used.

$$=P_{Dynamic} + P_{Short\ circuit} + P_{Leakage}$$

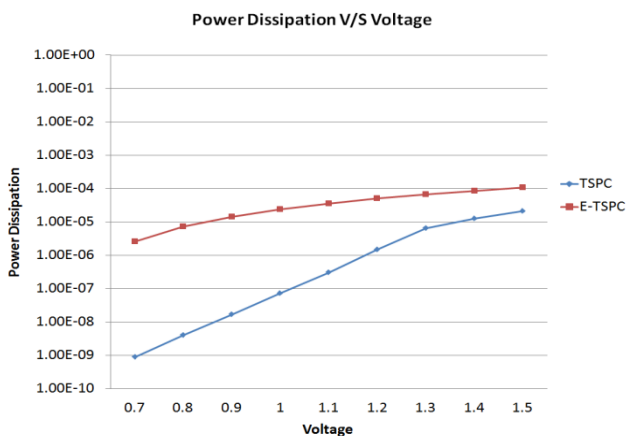


Figure 9: Power dissipation versus voltage comparison plot of TSPC and E-TSPC frequency divider.

4. Delay

In Digital electronics, the propagation delay, or gate delay, is the duration of time which is initiated when the input to a logic gate becomes stable and valid to transit, to the time that the output of that logic gate is stable and valid to transit. Often on manufacturers' datasheets this refers to the time needed for the output to go at 50% of its final output level when the input transits to 50% of its final input level. Reducing gate delays in digital circuits facilitates them to process data at a faster speed and improve overall circuit performance. The estimation of the propagation delay of a complex interconnect requires identification of the longest path of propagation delays from input to output and by superimposing each tpd time along this path. The delay is described in one sentence as the time taken by the circuit, from high to low or vice versa by a circuit is known as delay, the delay of CMOS circuitry is due to its internal capacitance generally represented as C_{ox} or oxide capacitance. it is represented by τ . This is calculated by

$$\tau = R_{MOS} C_{ox} \quad (2)$$

R_{MOS} is internal resistance of MOS devices and C_{ox} is capacitance of MOS transistor due to oxide layer with the help of SPICE delay at voltage level of 1 volt is 5.1236 ns. Here is plot of frequency divider circuitry using TSPC technique. Here we see certain increase in rising applied potential by 0.1 V. The circuit delay is very slightly increase which is less considerable in non-real time operation, while in real time application this delay can be completely optimized by counters and by using another techniques.

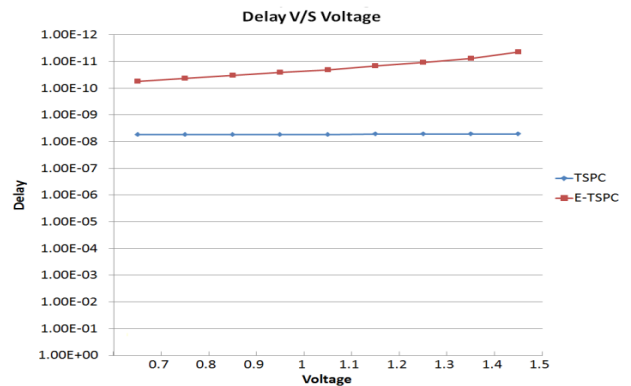


Figure 10 Delay versus voltage of TSPC and E-TSPC frequency divider comparison plot.

5. Power Delay Product

Even though the proposed 2 frequency divider divide by 2 with TSPC flip-flops acquires higher operating frequency; the higher power consumption leads to practically not preferable in mobile communications. Therefore it is better to choose proposed frequency divider divide by 2 with TSPC flip-flops for a 2 division. For further verification of the results and to come across a good comparison power-delay-product (PDP) of various frequency divider divide by 2s are found over different supply voltages in the range of .7 to 1.5 volts. For an efficient design, frequency divider divide by 2 having minimum power-delay product is preferred. Even though increasing the supply voltage reduces the operating circuit delay, it will increase the power consumption of device. Since frequency divider divide by 2s are

frequently used in mobile communications that is why power should be optimized. Therefore a circuit having minimum power delay product has to be chosen. The simulation results of power-delay-product symbolizes about the combined performance of speed and power, versus supply voltage for divide-by-2 TSPC Frequency Divider. Power Delay product[11] is nothing but energy consumed due to delay of circuit, greater the delay greater the power consumption wastage by the circuit.

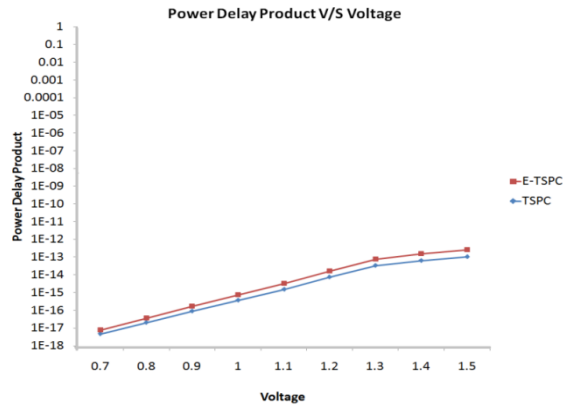


Figure 11: Power Delay product V/S Voltage comparison of TSPC and E-TSPC frequency divider

B. Analysis of Effects of variation in temperature

Now in this work we have noticed significant effects of temperature on frequency divider which is mainly due to semiconductor devices like MOSFETS used to design the TSPC and E-TSPC frequency divider circuit divide by 2 operation. We have simulated on 1V nominal voltage and varied temperature from 0 to 100 degree Celsius although this device can be work beyond 0 degree temperature, but power dissipation has to be compromise on such lower temperature. As wireless operations are done at various ambient temperatures at different geographical areas device so variation in temperature and dive operation is an important constraint to figure out. So these circuits have been simulated at various temperatures varying from -40 degrees to 1000 degrees centigrade for durability checking of this TSPC techniques based frequency divider circuit.

1. Power dissipation

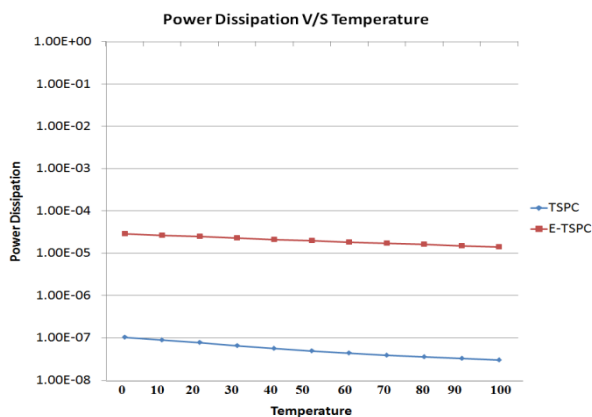


Figure 12: Power dissipation V/S Temperature comparison of TSPC and E-TSPC frequency divider.

Figure12 is plot of temperature versus power dissipation which is nearly a inverse logarithmic curve, it shows non linear behavior operation of device on rise is temperature, on higher temperature

device operation consumes low power. Leakage current and leakage power shows same variation plots and increase in temperature; both these parameters are increases exponentially as temperature is increased

2. Delay

Delay is significantly increases linearly but as temperature is increased, the slop of the graph will give the delay temperature coefficient by using slop determination techniques. As we have increased the temperature[11] of TSPC frequency divider delay of the circuit increases. But in reality at some minor level of changes in delay it has randomly increased at different temperatures.

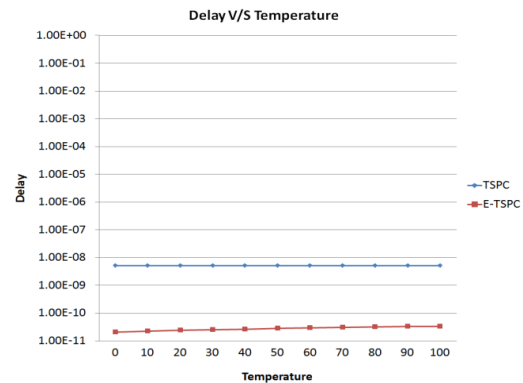


Figure 13: Delay V/S Temperature comparison of TSPC and E-TSPC frequency divider

CONCLUSION

From above analysis, it is observed that the TSPC has more delay then ETSPC based frequency divider i.e. TSPC technique based frequency dividers slower then E-TSPC frequency dividers. In case of forward body biasing circuit, the delay is low compare to other logic discussed here because of decrease in threshold voltage. ETSPC dividers have less delay and power delay product than the simple true single phase clock (TSPC). Therefore body biasing technique based extended true single phase clock (FBBETSPC) flip flop has better performance compare to TSPC dividers.

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