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CMOS 8-bit Counter for ADC Application

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***Abstract*—** In this paper design of synchronous 8-bit up counter is proposed. A counter can play an important role in several circuits such as in a simple display, microcontroller circuits etc. For counter, negative pulse-triggered master-slave D flip-flops is used. The negative pulse-triggered master-slave D flip-flops is implemented using DSCH software. Counter is designed with master-slave D flip-flop using Microwind software at 90nm technology.

Keywords*—Counter, Master-slave D flip-flop, microwind, DSCH.*

I. INTRODUCTION

Counter is a device which stores the number of times a particular event or process occurred, often in relationship to a clock signal. Counter is an essentially a register that goes through the predetermined sequence of states upon application of input pulses. Counter is a special type of register. A counter is a sequential machine that produces a specified count sequence [1]. The count changes whenever the input clock is asserted. Widest application of flip-flops is a Counter. A counter is useful in digital circuits. Counters are used in many applications for example to generate timing signals, to generate clocks of different frequencies. Counter is divided into synchronous and asynchronous types. In synchronous counter all flip-flops clocked at the same time, while asynchronous counter is not.

The proposed 8-bit synchronous up counter is implemented using microwind2 and DSCH software. The tool analyzes the performance of the design such as power, delay and area. Among those designs synchronous counters using master-slave D flip-flops have been widely used. In this paper we briefly explained 8-bit synchronous master slave D flip flop.

II. PROPOSED WORK

A. Master Slave D flip-Flop

A master-slave D flip-flop is implemented by connecting two gated D latches in series and inverting the enable input to one of them. The slave latch in the series only changes in response to a change in the first (master) latch so it is called as master-slave. The data is entered on the rising edge of the clock pulse, but output will be taken at the falling edge of the clock pulse. By using master-slave flip-flops a R-S, J-K, T or D flip-flop can be constructed. The master-slave configuration has the advantage of being pulse-triggered, making it easier to use in larger circuits, since the inputs to a flip-flop often depend on the state of its output [2].

Fig.1 shows pulse-triggered master-slave D flip-flop. This circuit will responds on the negative edge of a clock. Here two D flip-flops connected to each other. When the clock input is low, the first latch's output is stored in the second latch, but the first latch cannot change state. When the clock input is high, the D input is stored in the first latch, but the second latch cannot change state [5]. When the clock make the transition from high to low then only output can change state.

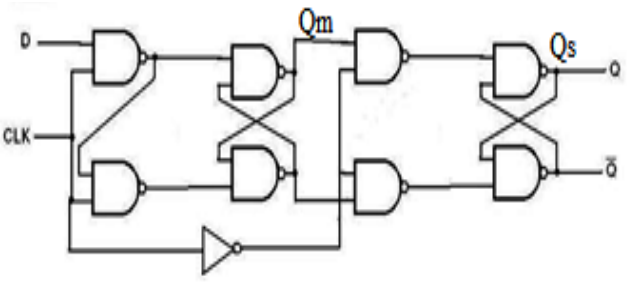

Figure 1: negative pulse triggered master slave D flip-flop

Table 1: Truth table of master-slave D flip-flop

Clk	Q_{n+1} (next state)
0	D
1	Q_n (present state)
X	0

B. Synchronous 8-Bit Up Counter

A Counter circuit is usually constructed of a number of flip flops connected in cascade. Each pulse applied to the clock input increments or decrements the number in the counter.

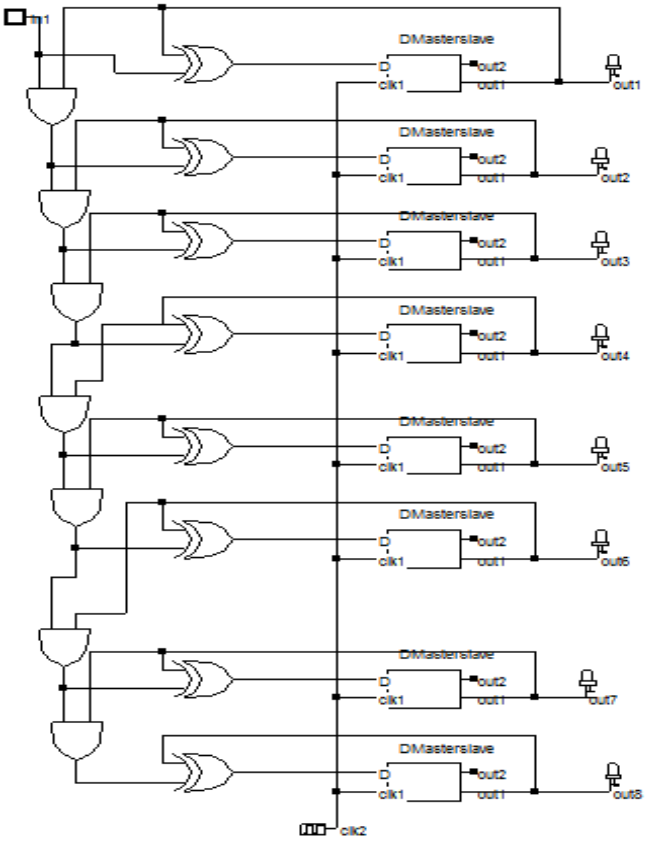

Figure 2: Synchronous 4-bit up counter

The master-slave D flip-flop actually works at the falling edge of the clock. But because it is a master slave configuration [8], it actually stores the input at rising edge and it is given to the output at the falling edge of the clock. So change in counter output is observed in the falling edge of the clock. It is an up counter. So it starts from 00000000, 00000001 to 11111111. Here input signal and clock signal is given to master slave D flip-flop. Internal diagram of master slave D flip-flop is shown in fig1. By using Fig.2 we get counted output.

III. SCHMATIC AND LAYOUT

For counter we use DSCH Software for Master-Slave D Flip-Flop. For layout of master slave flip-flop and 8-Bit up counter, we use microwind software.

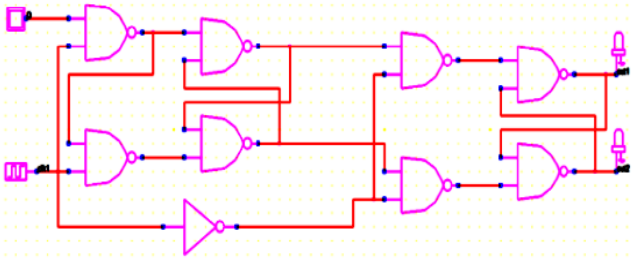

Figure 3: Master-slave D flip-flop schematic diagram

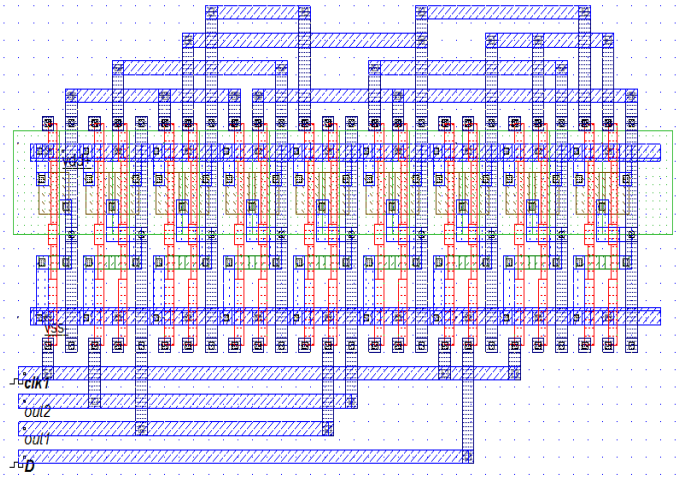

Figure 4: layout of Master-slave D flip-flop

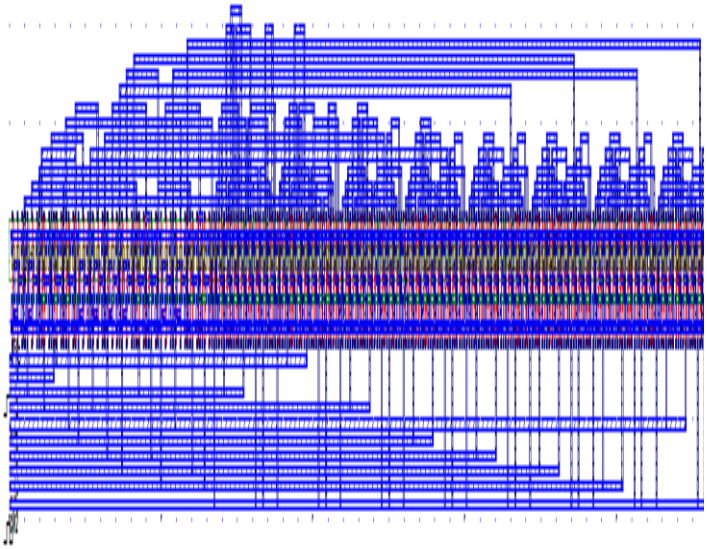

Figure 5: Layout of 8 bit counter

IV. SIMULATION RESULTS

Master slave D flip-flop change the state as shown in Table 1.

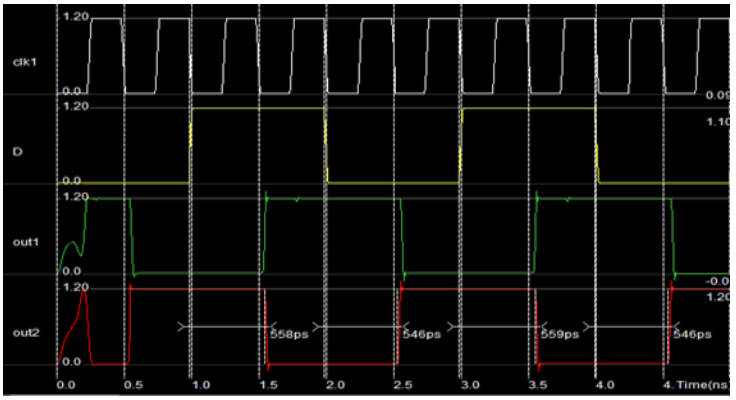

Figure 6: Result of Master-slave D flip-flop

Counter count on falling edge of clock signal

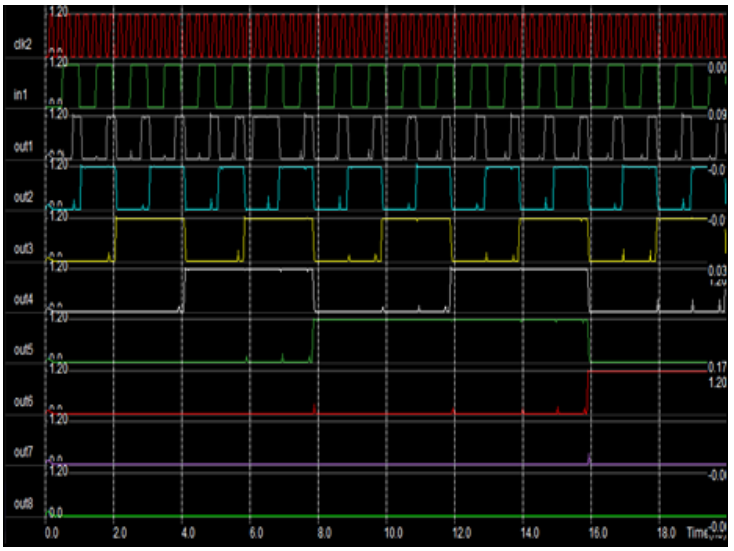

Figure 7: Result of 8 bit up counter

CONCLUSION

In this paper, synchronous 8-bit up counter has been implemented, simulated and analyzed. This 8-Bit synchronous up counter is used in ADC application. The performance of the counter is determined in terms of area and power consumption. The power used is 0.712mW for CMOS 90 nm process technology. The main goal to optimize the layout is met satisfactorily using DSCH and microwind software. Thus we present the design and implementation of synchronous 8-bit up counter which reduce the power supply and area.

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