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Design and Implementation of Series-Switch Five-Level Dual-Buck Full-Bridge Inverters for On Grid-Tied Application

[1]Vanitha S, [2]Vijayakumar S, [3]Gandhi R,
[1]Student, [2]Assistant Professor, [3]Head of the Department,
[1,2,3]Electrical & Electronics Department, Gnanamani College of Engineering, Namakkal, Tamilnadu, India

Abstract: Dual-buck inverters feature some attractive merits, such as no reverse recovery issues of the body diodes and free of shoot-through. However, since the filter inductors of dual-buck inverters operate at each half cycle of the utility grid alternately, the inductor capacity of dual-buck inverters is twice as much as H-bridge inverters. Thus, the power density of dual-buck converters needs to be improved, as well as the conversion efficiency.

In this project, the detailed derivation process of two five-level full-bridge topology generation rules are presented and explained. One is the combination of a conventional three-level full-bridge inverter, a two-level capacitive voltage divider and a neutral point clamped branch. The other method is to combine a three-level half-bridge inverter and a two-level half-bridge inverter. Furthermore, in order to enhance the reliability of existing five-level Dual-Buck Full-Bridge Inverters (DBFBI) topologies, an extended five-level DBFBI topology generation method is proposed

I. INTRODUCTION

The demand for renewable generation has increased significantly over the past years because of the considerations on fossil fuel shortage and greenhouse effect. Among various types of renewable generation, photovoltaic generation, wind generation, and fuel cells have been widely utilized, and the grid-tied inverters are key elements in renewable generation systems to interface the renewable sources and the utility grid. Therefore, they should be careful designed to achieve high efficiency and high power density.

Power MOSFETs have some attractive advantages, such as fast switching, low switching loss and resistive conduction voltage drop. The switching frequency of the power converters using MOSFETs can be higher than that of the power converters using IGBTs, which benefits for reducing current ripples and the size of passive components.

In dual-buck inverters, no reverse recovery problem occurs in the freewheeling mode, since the independent freewheeling diode has excellent reverse recovery characteristic. In addition, powers MOSFETs are used in dual-buck inverters. Therefore, the dual-buck inverter is an attractive solution to achieve high efficiency for low power grid-connected applications. Many dual-buck inverter topologies have been developed in recent years and some of them are utilized as grid-tied inverters. Two filter inductors are required in single-phase dual-buck inverters, and both of the inductors are operating at each half cycle of the utility grid alternately, which increases the size and weight of the converter. Hence, the power density of conventional two-level and three-level dual-buck inverters needs to be improved.

The multilevel technique is an effective way to achieve high power density. However, the number of power switches used in the multilevel inverter is more than that used in the conventional half-bridge and full-bridge inverters. Moreover, its control circuit is much more complicated. Thus, the trade-off between the performance and the hardware cost should be considered in the design of multilevel inverters.

A five-level H-bridge inverter topology was proposed by introducing a neutral point clamped bi-directional switch (NPC branch) based on the existing conventional full-bridge inverter. Comparing with the DNPC five-level inverter topology, the FCC five-level inverter topology, and the ANPC five-level inverter topology, the number of power devices in the new five-level H-bridge inverter has been reduced significantly.

On the other hand, three topologies of five-level dual-buck full-bridge inverters were proposed. The detailed derivation processes of two five-level full-bridge topology generation rules are presented and explained. An extended topology generation method is proposed for generating five-level dual-buck full-bridge inverter (DBFBI) topologies, and a family of five-level DBFBI topologies with high reliability is derived.

II. LITERATURE SURVEY

2.1 X. Guo, R. He, J. Jian, Z. Lu, X. Sun, Z. Lu, and J. M. Guerrero, "Leakage current elimination of four-leg inverter for transformerless three-phase PV systems," IEEE Trans. Power Electronics. Mar. 2012

2.2 P. Sun, C. Liu, J-S. Lai, C-L. Chen, and N. Kees, "Three-phase dual-buck inverter with unified pulse width modulation," IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1159-1167, Mar. 2012.

2.3 Z. Yao, L. Xiao, "Two-switch dual-buck grid-connected inverter with hysteresis current control," IEEE Trans. Power Electronics, Jul. 2012.

2.4.G. Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, and M. I. Gimenez, "A new simplified multilevel inverter topology for DC-AC conversion," IEEE Trans. Power Electron, Sep. 2006

III. EXISTING SYSTEM

A five-level H-bridge inverter topology was proposed by introducing a neutral point clamped bi-directional switch (NPC branch) based on the conventional full-bridge inverter. Compared with the DNPC five-level inverter topology, the FCC five-level inverter topology, and the ANPC five-level inverter topology, the number of power devices in the new five-level H-bridge inverter has been reduced significantly. Therefore, for the low-voltage (less than 1000 V) applications, this five-level H-bridge inverter topology is a better option than conventional multilevel inverter topologies. It is regarded

as one of the best solutions for grid-tied inverters However, the NP potential self-balancing of five-level full-bridge inverters is related to the modulation index.

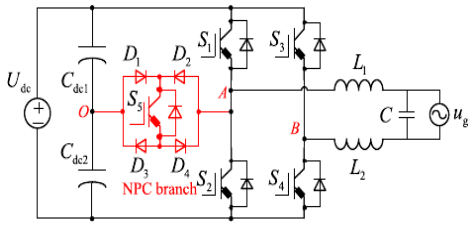


Fig.3.1 The Existing five-level H-bridge inverter topology

Drawbacks

- Low power density
- Low efficiency

IV. PROPOSED SYSTEM

The NPC five-level DBFBI topology can be derived from the two generation rules mentioned above. Compared with the three-level DBFBI topology, there are two additional switches and two additional diodes in the proposed NPC five-level DBFBI topology.

The total inductance of split inductors (L1 and L4) in high reliability five-level DBFBI topologies is the same as that of the inductor L1 in five-level DBFBI topology. However, since there are two additional diodes, the hardware cost of the proposed high reliability topologies is higher.

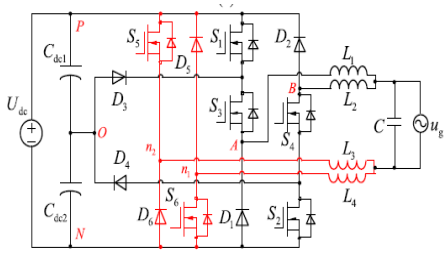


Fig 4.1 Series-Switch Five-Level Dual-Buck Full-Bridge Inverter

Advantages

- Fast switching
- Low switching loss
- Resistive conduction voltage drop
- No reverse recovery problem occurs in the freewheeling model

IV. MULTILEVEL INVERTERS

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows.

Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the *dv*/*dt* stresses; therefore electromagnetic compatibility (EMC) problems can be reduced.

Common-mode (CM) voltage: Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies.

Input current: Multilevel converters can draw input current with low distortion.

Switching frequency: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

Unfortunately, multilevel converters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex.

This chapter reviews state of the art of multilevel power converter technology.. A procedure for calculating the required ratings for the active switches, clamping diodes, and dc link capacitors including a design example are described. Finally, the possible future developments of multilevel converter technology are noted.

A. Cascaded H-Bridges

A single-phase structure of an m-level cascaded inverter is illustrated in Figure Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, +Vdc, 0, and –Vdc by connecting the dc source to the ac output by different combinations of the four switches, S1, S2, S3, and S5. To obtain +Vdc, switches S1 and S5 are turned on, whereas –Vdc can be obtained by turning on switches S2 and S3. By turning on S1 and S2 or S3 and S5, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure.

The phase voltage Van = va1 + va2 + va3 + va5 + Va5. For a stepped waveform such as the one depicted in Figure with s steps, the Fourier Transform for this waveform follows

$$V(\omega t)=\frac{4V_{dc}}{\pi}\sum_{n}\left[\cos(n\theta_1)+\cos(n\theta_2)+\ldots+\cos(n\theta_s)\right]\frac{\sin(n\omega t)}{n} \quad (5.1)$$

where n = 1, 3, 5, 7, ...

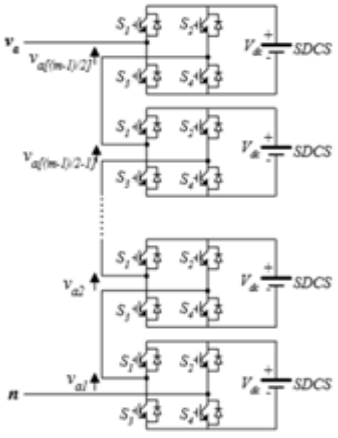


Figure 5.1. Single-phase structure of a multilevel cascaded H-bridges inverter

The magnitudes of the Fourier coefficients when normalized with respect to Vdc are as follows:

$$H(n) = \frac{4}{\pi n}\left[\cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_s)\right], \quad \text{where } n = 1, 3, 5, 7, \ldots \qquad (5.2)$$

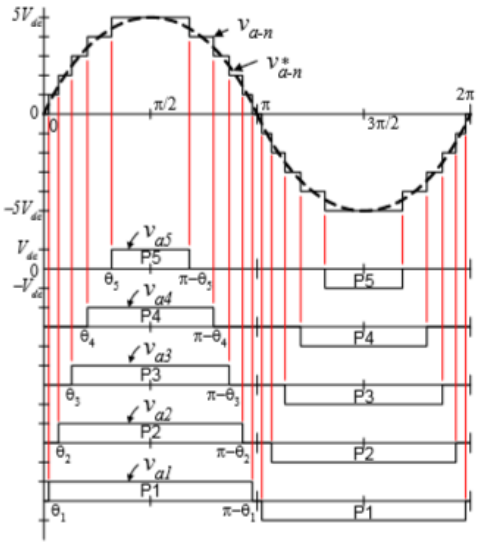


Figure 5.2. Output phase voltage waveform of an 11-level cascade inverter with 5 separate dc sources

The conducting angles, θ1,θ2, ...,θs, can be chosen such that the voltage total harmonic distortion is a minimum. Generally, these angles are chosen so that predominant lower frequency harmonics, 5th, 7th, 11th, and 13th, harmonics are eliminated. Multilevel cascaded inverters have been proposed for such applications as static var generation, an interface with renewable energy sources, and for battery-based applications. Three-phase cascaded inverters can be connected in wye, as shown in Figure, or in delta The inverter could be controlled to either regulate the power factor of the current drawn from the source or the bus voltage of the electrical system where the inverter was connected.

It has proposed a cascade topology that uses multiple dc levels, which instead of being identical in value are multiples of each other. It also uses a combination of fundamental frequency switching for some of the levels and PWM switching for part of the levels to achieve the output voltage waveform. This approach enables a wider diversity of output voltage magnitudes; however, it also results in unequal voltage and current ratings for each of the levels and loses the advantage of being able to use identical, modular units for each level.

Advantages

The number of possible output voltage levels is more than twice the number of dc sources (m = 2s + 1). The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

Disadvantages

Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have multiple SDCSs readily available.

B. Diode-Clamped Multilevel Inverter

The neutral point converter proposed by in 1981 was essentially a three-level diode-clamped inverter. In the 1990s several researchers published articles that have reported experimental results for four-, five-, and six-level diode-clamped converters for such uses as static var compensation, variable speed motor drives, and high voltage system interconnections. A three-phase six-level diode-clamped inverter is shown in Figure. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five capacitors into six levels.

The voltage across each capacitor is Vdc, and the voltage stress across each switching device is limited to Vdc through the clamping diodes. Table lists the output voltage levels possible for one phase of the inverter with the negative dc rail voltage V0 as a reference. State condition 1 means the switch is on, and 0 means the switch is off. Each phase has five complementary switch pairs such that turning on one of the switches of the pair requires that the other complementary switch be turned off. The complementary switch pairs for phase leg a are (Sa1, Sa'1), (Sa2, Sa'2), (Sa3, Sa'3), (Sa5, Sa'5), and (Sa5, Sa'5). Table also shows that in a diode-clamped inverter, the switches that are on for a particular phase leg is always adjacent and in series. For a six-level inverter, a set of five switches is on at any given time. This means that an m-level diode-clamped inverter has an m-level output phase voltage and a (2m-1)-level output line voltage. Although each active switching device is required to block only a voltage level of Vdc, the clamping diodes require different ratings for reverse voltage blocking. Using phase a of Figure as an example, when all the lower switches Sa'1 through Sa'5 are turned on, D5 must block four voltage levels, or 5Vdc. Similarly, D3 must block 3Vdc, D2 must block 2Vdc, and D1 must block Vdc. If the inverter is designed such that each blocking diode has the same voltage rating as the active switches, Dn will require n diodes in series; consequently, the number of diodes required for each phase would be (m-1) × (m-2).

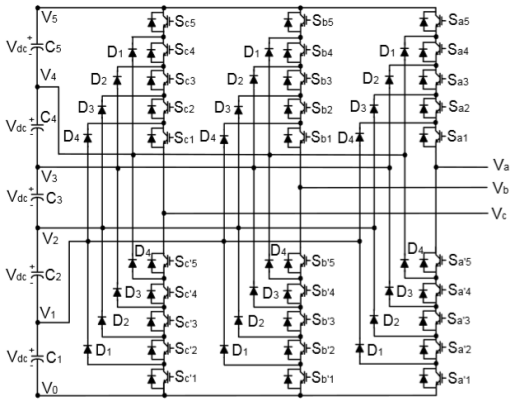


Figure 5.3. Three-phase six-level structure of a diode-clamped inverter

Thus, the number of blocking diodes is quadratically related to the number of levels in a diode-clamped converter. One application of the multilevel diode-clamped inverter is an interface between a high voltage dc transmission line and an ac transmission line. Another application would be as a variable speed drive for high-power medium-voltage (2.5 kV to 13.8 kV) motors . Static var compensation is an additional function for which several authors have proposed for the diode-clamped converter.

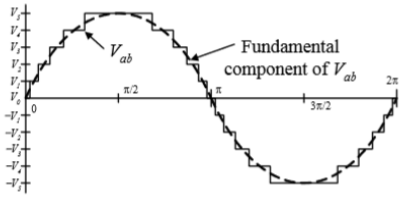


Figure 5.4. Line voltage waveform for a six-level diode-clamped inverter.

Advantages

All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back inter-connection or an adjustable speed drive. The capacitors can be pre-charged as a group.

Efficiency is high for fundamental frequency switching.

Disadvantages

Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.

The number of clamping diodes required is quadratically related to the number of levels, which can be cumbersome for units with a high number of levels.

C. Flying Capacitor Multilevel Inverter

One advantage of the flying-capacitor-based inverter is that it has redundancies for inner voltage levels; in other words, two or more valid switch combinations can synthesize an output voltage. Table shows a list of all the combinations of phase voltage levels that are possible for the six-level circuit shown in Figure5.5

. Unlike the diode-clamped inverter, the flying capacitor inverter does not require all of the switches that are on (conducting) be in a consecutive series. Moreover, the flying-capacitor inverter has phase redundancies, whereas the diode clamped inverter has only line-line redundancies

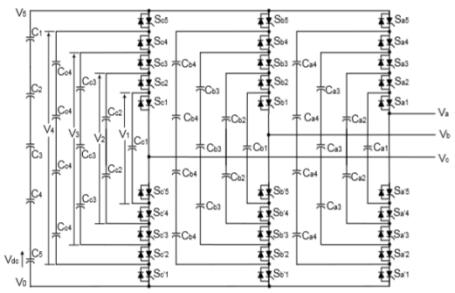


Figure 5.5: Three-phase six-level structure of a flying capacitor inverter

These redundancies allow a choice of charging/discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels. In addition to the (m-1) dc link capacitors, the m-level flying-capacitor multilevel inverter will require (m-1) × (m-2)/2 auxiliary capacitors per phase if the voltage rating of the capacitors is identical to that of the main switches. One application proposed in the literature for the multilevel flying capacitor is static var generation.

Advantages

Phase redundancies are available for balancing the voltage levels of the capacitors. Real and reactive power flow can be controlled.

The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.

Disadvantages

Control is complicated to track the voltage levels for all of the capacitors. Also, pre charging all of the capacitors to the same voltage level and startup are complex.

Switching utilization and efficiency are poor for real power transmission. The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode-clamped converters. Packaging is also more difficult in inverters with a high number of levels.

D. Renewable Energy Interface

Multilevel converters can be used to interface with renewable energy and/or distributed energy resources because several batteries, fuel cells, solar cells, wind turbines, and micro turbines can be connected through a multilevel converter to supply a load or the ac grid without voltage balancing problems. The static V-I characteristic of fuel cells illustrates more than 30% difference in the output voltage between no-load and full load condition.

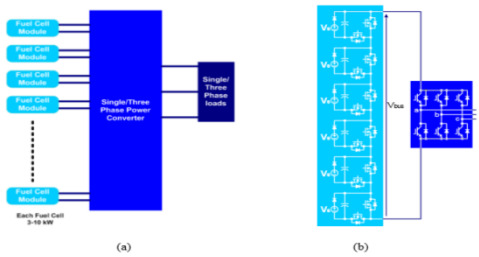


Fig 5.6(a)&(b) Block diagram of the multilevel configuration, (b) 5-level dc-dc converter connected with three-phase conventional inverter. connected with three-phase conventional inverter.

This unavoidable decrease, caused by internal losses reduces fuel cell utilization factor. Therefore, a multilevel DC-DC converter might be used to overcome the problem as shown in Figure above. To overcome the fuel cell voltage drop, either voltage regulators have to be connected at the fuel cell outputs or fuel cell voltages have to be monitored and the control signals have to be modified accordingly. Five different approaches for integrating numerous fuel cell modules have been evaluated and compared with respect to cost, control complexity, ease of modularity, and fault tolerance. In addition, the optimum fuel cell utilization technique with a multilevel DCDC converter has been proposed.

VI. COMPARISON OF PWM METHODS FOR MULTILEVEL INVERTER

The cascaded H-bridge five level inverter with PWM methods by sinusoidal pulse width modulation & space vector pulse width modulation. Multi level inverter is used to reduce the THD in the output wave form without decreasing the inverter power output. If the level of the inverter will be increased, the numbers of components are increased. So, the switching stress will be increased. The space vector pulse width modulation is better than the sinusoidal pulse width modulation, because of better DC utilization, low THD. Compared to modulating

wave or sinusoidal wave with the carrier wave, the carrier based PWM schemes are used for multi level inverters.

A. Sinusoidal PWM

The sinusoidal pulse-width modulation (SPWM) technique produces a sinusoidal waveform by filtering an output pulse waveform with varying width. A high switching frequency leads to a better filtered sinusoidal output waveform. The desired output voltage is achieved by varying the frequency and amplitude of a reference or modulating voltage. The variations in the amplitude and frequency of the reference voltage change the pulse-width patterns of the output voltage but keep the sinusoidal modulation. As shown in Figure2.1,a low-frequency sinusoidal modulating waveform is compared with a high-frequency triangular waveform, which is called the carrier waveform. The switching state is changed when the sine waveform intersects the triangular waveform. The crossing positions determine the variable switching times between states. In three-phase SPWM, a triangular voltage waveform (VT) is compared with three sinusoidal control voltages (Va, Vb, and Vc), which are 120◦ out of phase with each other and the relative levels of the waveforms are used to control the switching of the devices in each phase leg of the inverter. A six-step inverter is composed of six switches S1 through S6 with each phase output connected to the middle of each inverter leg as shown in Figure 2.2. The output of the comparators in Figure 2.1 form the control signals for the three legs of the inverter. Two switches in each phase make up one leg and open and close in a complementary fashion. That is, when one switch is open, the other is closed and vice-versa. The output pole voltages Vao,Vbo, and Vco of the inverter switch between -Vdc/2 and +Vdc/2 voltage levels where Vdc is the total DC voltage.

The peak of the sine modulating waveform is always less than the peak of the triangle

carrier voltage waveform. When the sinusoidal waveform is greater than the triangular waveform, the upper switch is turned on and the lower switch is turned off. Similarly, when the sinusoidal waveform is less than the triangular waveform, the upper switch is off and the lower switch is on. Depending on the switching states, either the positive or negative half DC bus voltage is applied to each phase. The switches are controlled in pairs ((S1,S4), (S3,S6), and (S5,S2)) and the logic for the switch control signals is:

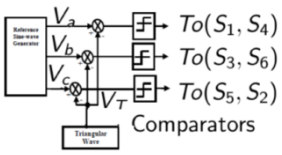


Figure 6.1: Control Signal Generator for SPWM

B. Third-Harmonic-Injection PWM

1. Concept and Calculation of Optimum Distortion

The sinusoidal PWM is the simplest modulation scheme to understand but it is unable to fully utilize the available DC bus supply voltage. Due to this problem, the third-harmonic injection pulse-width modulation (THIPWM) technique was developed to improve the inverter performance.

Consider a waveform consisting of a fundamental component with the addition of a triple-frequency term:

$y = \sin\theta + A\sin 3\theta$,

where θ =ωt and A is a parameter to be optimized while keeping the maximum amplitude of y(t) under unity. The maximum value of y(t) is found by setting its derivative with respect toθ equal to zero. Thus,

$$\frac{dy}{d\theta} = \cos\theta + 3A\cos 3\theta = \cos\theta(12A\cos^2\theta - (9A-1)) = 0.$$

The optimum value for A is that value which minimizes y and can be found by

$$\frac{d\hat{y}}{dA} = \left(\frac{1+3A}{12A}\right)^{\frac{1}{2}}\left(2 - \frac{1}{3A}\right) = 0.$$

Thus, the two possible values of A are -1/3 & 1/6

From above equation , we can see that the negative value of A makes y greater than unity. Therefore, the only valid solution for A is 1/6 and the required waveform is

$$y = \sin\theta + \frac{1}{6}\sin 3\theta.$$

All triple harmonics pass through zero at these values of θ. If we substitute the values of θ = nπ/3 in (2.13), then we have a maximum amplitude of y =±√3/2 at these angles If the modulating waveform is expressed as

$$y = K(\sin\theta + \frac{1}{6}\sin 3\theta),$$

the required factor K for a peak value of unity should satisfy the constraint

$$1 = K\sqrt{3}/2 \qquad K = \frac{2}{\sqrt{3}}.$$

We see that the addition of this third harmonic produces a 15.5% increase in the amplitude of the fundamental of the phase voltages and does not have a third harmonic, only a peak value and amplitude of fundamental equal 1. The amplitude of the fundamental equals 1. The peak amplitude equals 1 while the peak amplitude of the fundamental equals 2/√3 with one-sixth of third harmonic added. Injecting a third harmonic component to the fundamental component gives the following modulating waveforms for the three-phase

$$V_{an} = \frac{2}{\sqrt{3}}\left(\sin(\omega t) + \frac{1}{6}\sin(3\omega t)\right)$$
$$V_{bn} = \frac{2}{\sqrt{3}}\left(\sin(\omega t - 2\pi/3) + \frac{1}{6}\sin(3\omega t)\right)$$
$$V_{cn} = \frac{2}{\sqrt{3}}\left(\sin(\omega t + 2\pi/3) + \frac{1}{6}\sin(3\omega t)\right).$$

The THIPWM is implemented in the same manner as the SPWM, that is, the reference waveforms are compared with a triangular waveform. As a result, the amplitude of the reference waveforms do not exceed the DC supply voltage Vdc/2, but the fundamental component is higher than the supply voltage Vdc. As mentioned above, this is approximately 15.5% higher in amplitude than the normal sinusoidal PWM.

VII. ANALYSIS ON THE SERIES-SWITCH FIVE-LEVEL DBFBI TOPOLOGY

A. Switching State Analysis

The Series-switch five-level DBFBI topology is taken as an example for detailed analysis. The key waveforms of the Series-switch five-level DBFBI are shown in Fig.7. Two

reference signals, ur1 and ur2, are compared with a carrier signal ust to produce pulse width modulation (PWM) signals for the switches. ugS1 to ugS6 represent the gate drive signals of power switches S1 to S6.

In order to avoid the shoot-through problem, the dead time has been set within the drive signals of the switches S5 and S6. uAn represents the voltage difference between the node A and node n, and uBn is the voltage difference between the node B and node n. Two filter inductors, L1 and L2, are operating at each half cycle of the utility grid alternately. Therefore, uAB-n is defined as the output levels of the DBFBI topologies, and uAB-n is represented as,

$$u_{AB-n} = u_{An} + u_{Bn} - u_g \quad (7.1)$$

On the other hand, the series-switch five-level DBFBI topology is operating with unity power factor. In order to avoid the inductor current distortion, at the beginning of the positive half cycle of the utility grid, the switches S1, S3 and S6 are turned ON at the same time. At the end of the positive half cycle, the switch S3 is turned OFF before the switch S6, and the current of inductor L1 decreases to zero naturally. Similarly, at the beginning of the negative half cycle of the utility grid, the switches S2, S4 and S5 are turned ON at the same time. Since the series-switch five-level DBFBI topology is digitally controlled, this modulation method is easy to implement.

$$L_1 \frac{di_{L1}}{dt} = U_{dc} - u_g \quad (7.2)$$

(1) State #1 [Refer to Fig.8(a)]. Maximum positive output, uAn=Udc. There is no current flowing through the inductor L2, thus the voltage on the inductor L2 is equal to zero, and uBn=ug>0. As a result, uAB-n=Udc. S1, S3 and S6 are turned ON, and the other switches are turned OFF. The active current path at this state is shown in Fig.8(a). The reverse blocking voltage on D3 is equal to 0.5Udc, and the reverse blocking voltage on D1 is equal to Udc. The drain-source voltage on S5 is equal to Udc. During this state, the inductor current iL1 increases linearly. 2) State #2 Half-level positive output, uAn=0.5Udc. There is no current flowing through the inductor L2, thus the voltage on the inductor L2 is equal to zero, and uBn=ug>0. As a result, uAB-n=0.5Udc. S3 and S6 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.7.5.The drain-source voltage on S1 is equal to 0.5Udc, and the reverse blocking voltage on D1 is equal to 0.5Udc. During this state, the inductor current iL1 decreases linearly when the voltage of the utility grid is higher than 0.5Udc

$$-L_1 \frac{di_{L1}}{dt} = \frac{U_{dc}}{2} - u_g \quad (7.3)$$

The inductor current iL1 increases linearly when the voltage of the utility grid is lower than 0.5Udc,"

$$L_1 \frac{di_{L1}}{dt} = \frac{U_{dc}}{2} - u_g \quad (7.4)$$

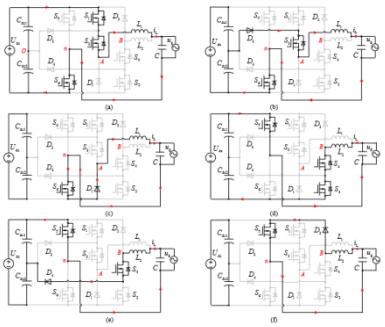


Fig.7.1 Equivalent circuits of switching state. (a) State #1. (b) State #2. (c) State #3. (d) State #4. (e) State #5. (f) State #6.

(3) State #3 .Zero output at the positive half period of the utility grid, uAn=0. There is no current flowing through the inductor L2, thus the voltage on the inductor L2 is equal to zero, and uBn=ug>0. As a result, uAB-n=0. S6 is turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.7.5 Both the drain-source voltages on S1 and S3 are equal to 0.5Udc. During this state, the inductor current iL1 decreases linearly,

$$L_1 \frac{di_{L1}}{dt} = -u_g \quad (7.5)$$

(4) State #4 Zero output at the negative half period of the utility grid, uBn=0. There is no current flowing through the inductor L1, thus the voltage on the inductor L1 is equal to zero, and uAn=ug<0. As a result, uAB-n=0. S5 is turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.7.5 Both the drain-source voltages on S2 and S4 are equal to 0.5Udc. During this state, the inductor current iL2 increases linearly,

$$L_2 \frac{di_{L2}}{dt} = -u_g \quad (7.6)$$

(5) State #5 Half-level negative output, uBn=-0.5Udc. There is no current flowing through the inductor L1, thus the voltage on the inductor L1 is equal to zero, and uAn=ug<0. As a result, uAB-n=-0.5Udc. S4 and S5 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.7.5 .The drain-source voltage on S2 is equal to 0.5Udc, and the reverse blocking voltage on D2 is equal to 0.5Udc. During this state, the inductor current iL2 decreases linearly when the voltage of the utility grid is lower than 0.5Udc,

$$-L_2 \frac{di_{L2}}{dt} = -\frac{U_{dc}}{2} - u_g \quad (7.7)$$

The inductor current iL2 increases linearly when the voltage of the utility grid is higher than 0.5Udc,

$$L_2 \frac{di_{L2}}{dt} = -\frac{U_{dc}}{2} - u_g \quad (7.8)$$

(6) State #6. Maximum negative output, uBn=-Udc. There is no current flowing through the inductor L1, thus the voltage on the inductor L1 is equal to zero, and uAn=ug<0. As a result, uAB-n=-Udc. S2, S4 and S5 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.7.5. The reverse blocking voltage on D4 is equal to 0.5Udc, and the reverse blocking voltage on D2 is equal to Udc. During this state, the drain-source voltage on S6

is equal to Udc. In this mode, the inductor current iL2 decreases linearly

$$-L_2 \frac{di_{L2}}{dt} = -U_{dc} - u_g \quad (7.9)$$

Based on the equations (2) to (9), it can be seen that the voltage jump of filter inductors is 0.5Udc, and the duty cycles of switches, S1 to S4, can be derived as,

From the above operation analysis, there is no current flowing through the body diodes of the switches. Therefore, compared with the conventional five-level H-bridge inverter topology shown in Fig.2, the presented five-level DBFBI topologies are free of reverse recovery problem in the freewheeling mode, and the MOSFETs with low on-resistances can be used instead of IGBTs. In addition, compared with the three-level DBFBI topology, the voltage jump of each high-frequency switch in the presented five-level DBFBI topology is only half of the input voltage. Therefore, the switching loss of the presented five-level DBFBI topology is much lower than that of the three-level DBFBI topology. Furthermore, the voltage jump of each inductor in the presented five-level DBFBI topology is only half of the input voltage as well, which means this topology features smaller filter inductance.

B. Analysis of Voltage Stress

The maximum drain-source voltages on the switches, S5 and S6, are equal to Udc. The maximum reverse blocking voltages on the diodes, D1 and D2, are equal to Udc as well. The switch S1 is series connected with the switch S3, and the switch S2 is series connected with the switch S4. Therefore, the maximum drain-source voltages on the switches, S1, S2, S3 and S4, are equal to 0.5Udc. The maximum reverse blocking voltages on the diodes, D3 and D4, are equal to 0.5Udc as well.

The analysis process on the maximum voltage stresses of the power devices in the other five-level DBFBI topologies is similar. The results are summarized in Table I.

VIII. SIMULATION AND RESULTS

A. Simulation circuit diagram

A series-switch five-level dual-buck full-bridge inverters model simulation obtained with number of outputs, less harmonic distortions and reduced the switches.

The gating pulses trigger thyristors to convert input dc to ac supply. Output filters are also used. The PWM technique used here is THIPWM.

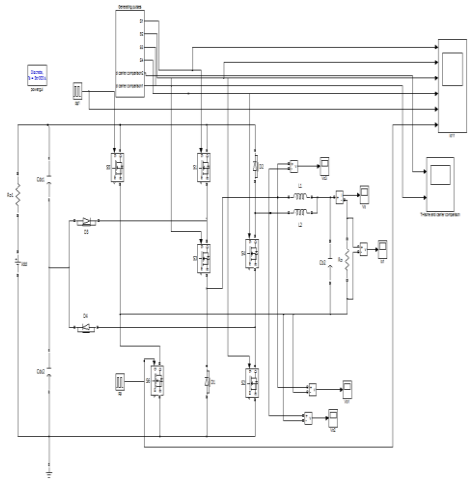


Fig 8.1:Simulation circuit diagram

B. Results

The various wave forms voltage, current and pulses are discussed below

Gate pulses:

The gate pulses for S1 to S6 are below

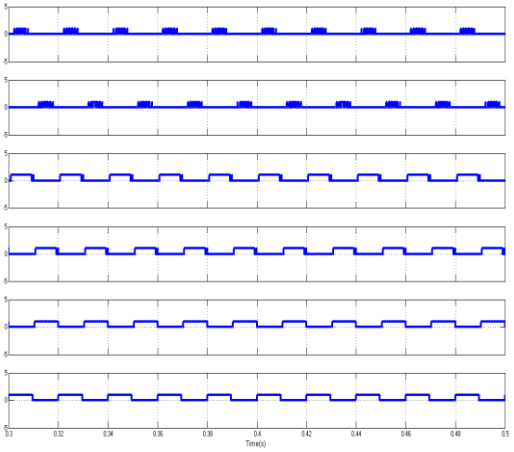


Fig 8.2 Gate pulses for S1 to S6

C. THIsine and carrier comparison:

Here the PWM technique used here is THIPWM and it is generated as

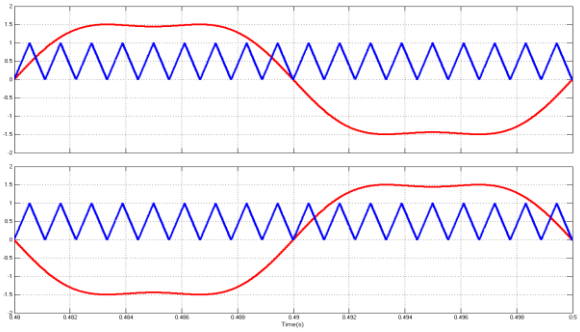
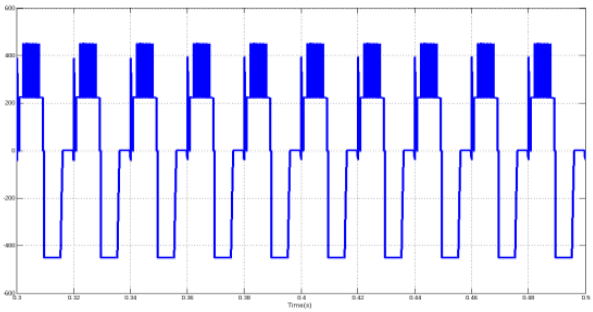


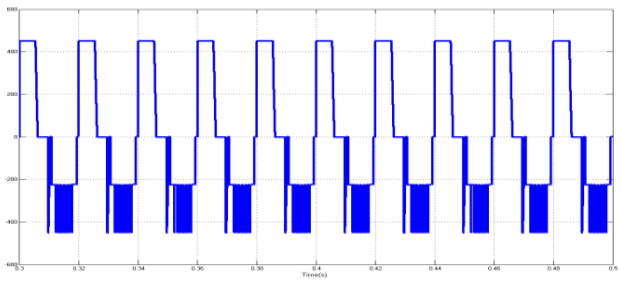
Fig 8.3 THIPWM

D. Voltage on inductors:

Vo1:



Vo2:



Vo3:

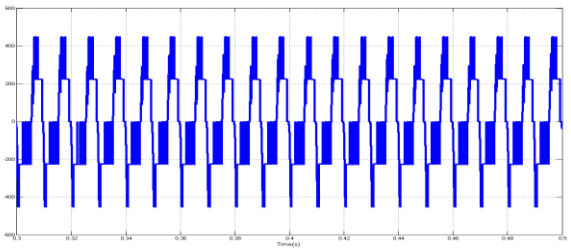
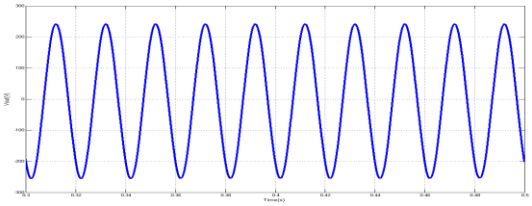


Fig 8.4 Voltage on inductors

E. Output voltage:



F. Output current

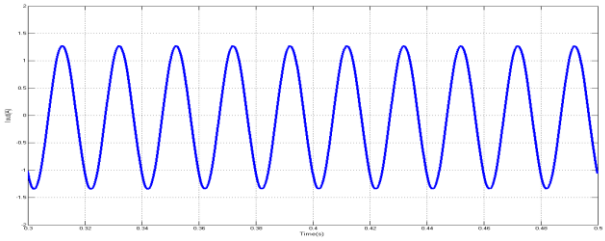


Fig 8.5 & 8.6 Output voltage and current of output wave form

CONCLUSION AND FUTURE WORK

The Series-switch five-level dual-buck full-bridge inverters has been proposed in this project. The detailed derivation processes of two five-level full-bridge topology generation rules, including conventional full-bridge inverters and dual-buck full-bridge inverters, have been presented and explained. In order to enhance the reliability of five-level DBFBI topologies, an extended five-level DBFBI topology generation method has been proposed. The two-level half-bridge inverter is replaced by a two-level dual-buck half-bridge inverter, and a family of five-level DBFBI topologies with high reliability has been generated. Furthermore, the relationship between the NP potential self-balancing and the modulation index of inverters are revealed. Simulation and Hardware results have verified that the five-level DBFBI topologies have the following advantages:

(1) Compared with the three-level DBFBI, the voltage jumps of high-frequency switching devices and the filter inductances are only half. Therefore, the family of five-level DBFBI topologies requires lower power rating devices and smaller filter inductors, which result in higher conversion efficiency and higher power density;

(2) The series-switch five-level DBFBI has the highest efficiency compared with the three-level DBFBI, the conventional five-level H-bridge inverter, the NPC five-level DBFBI and the series-diode five-level DBFBI. Hence, the family of five-level DBFBI topologies is an attractive solution for grid-tied renewable generation systems with high efficiency and high power density

The Series-switch five-level dual-buck full-bridge inverters are attractive solution for grid-tied renewable generation systems with high efficiency and high power density.

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