International Journal of Trend in Research and Development, Volume 4(1), ISSN: 2394-9333
www.ijtrd.com

64 Bit SRAM Design using 5T and a Comparative Study between 6T and 5T Designs

[1]Nitin Tiwari and [2]Amit Mishra
[1,2]Department of Electronics and Communication, Vindhya Institute of Technology & Science, Jabalpur, M. P., India

***Abstract*—** The main goals of NLSI Designer are to reduce the area, improve performance and decreasing the cost. There are several sources for the leakage current, i.e. low threshold voltage causes to sub-threshold current, very thin gate oxides cause to gate leakage, and heavily-doped halo doping profile causes to band-to-band tunneling leakage. It is seemed that we have to focus to minimize the leakage power in the number of transistors and the large memory substance of future SoC (System on Chip) devices [4].

***Keywords*—** *Memory, tunneling leakage, Systems-on-Chip, leakage power consumption.*

I. INTRODUCTION

SRAM is the building block of several logic circuits. SRAM is a very fast and low power memory. It is essential to understanding how an SRAM is work and how it designs for building any advanced logic circuits. Using this knowledge and experience, we can design more complex integrated circuits. For designing the SRAM we will follow the principle "Computer Hardware" Which uses a modular design that lies of smaller, more manageable blocks, some of which can be re-used and also designed by the bottom-up methodology [7].

A. Power Dissipation in CMOS

There are 3 components which are responsible for power consumption-

1. Static power
2. Dynamic power
3. Short circuit power

CMOS power consumption contains static and dynamic components [5]. Static power consumption is very low and it is the result of the leakage current. Dynamic power or switching power is mainly power dissipated when charging or discharging capacitors. When all inputs are held at some valid logic level and the circuit is not in charge states then this power consumption occurs. It increases by charging and discharging output capacitance. It can significantly contribute to the overall power consumption if switching at a frequency [6].

B. SRAM Design

H. Mangalam - This paper shows that in the deep submicron regimes the high leakage current may be majorly contribute to the total power consumption in CMOS circuits as the channel length, thickness of the gate oxide and threshold voltage. This paper proposed an Asymmetric SRAM (SA) cell with the extra transistor that reduced the gate leakage as compared to the conventional 6T SRAM cell. Further to reduce the leakage an Adaptive voltage level was added that controlled the effective voltage across SRAM cell in the inactive mode. 2 methods were employed-

1. In the 1st method the supply voltage is reduced.
2. In the 2nd method the ground potential was increased.

SPICE Simulations are performed with 130nm CMOS technology process file and the leakage currents of all the cells are measured and compared.

C. 5T 1 bit SRAM

a. Flow Chart for 5T bit SRAM

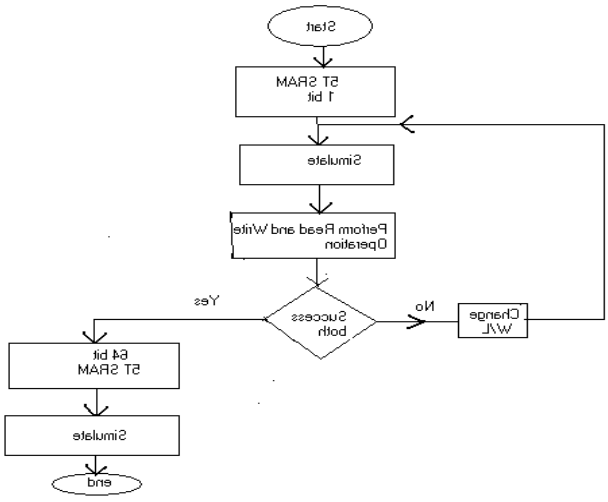

Figure 1: Flow Chart for 5T SRAM

b. 5T 1 bit SRAM

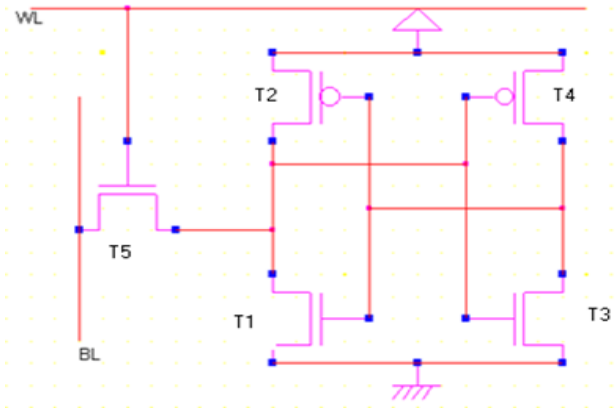

Figure 2: 5T 1Bit SRAM (proposed)

The three different states work as follows –

When the WL is not asserted, the access transistor disconnects the cell from the BL. There are 2 cross coupled invertors and will continue to support together as long as they are supplied. Assume that the content of the memory is a 1, stored at Q.

Now read cycle is started by pre-charging the BL to logic 1, then asserting the WL enables the access transistor. Next step occurs when the values started in Q and $\overline{Q}$ are transferred to the BL by leaving BL at its pre- charged value. If the content of the memory were a 0, the opposite would happen .The start of a write cycle begins by applying the value to be written to the bit line. If we wish to write a 0, we would apply a 0 to the bit line, i.e. BL to 0. This is similar to applying a reset pulse to a SR-latch, which causes the flip flop to change state. Then WL asserted and the value which is to be stored is latched in.

c. 1-Bit SRAM

Here we design a schematic of SRAM cell by DSCH2 Software and implemented it by Microwind 3.1. This design has been simulated by CMOS technology. Now we design 64 bits SRAM by using 5T SRAM cell and compare the result with conventional 6T SRAM cell structure. The transistors reduce dynamic power consumption during write operation through proper charging and discharging of the bit lines.

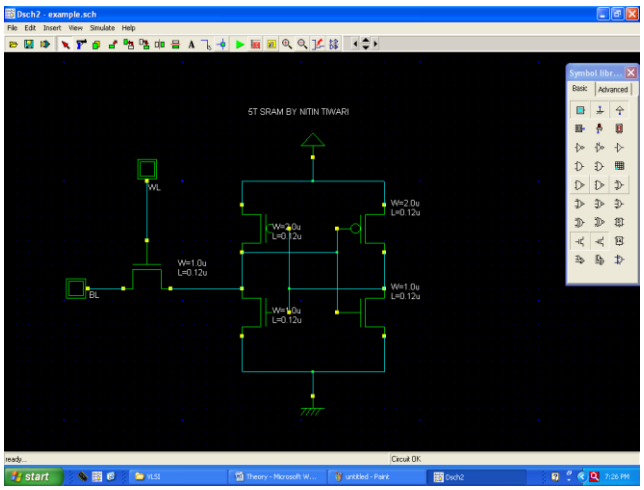

Figure 3:Schematic of 5T 1-Bit SRAM by DSCH2

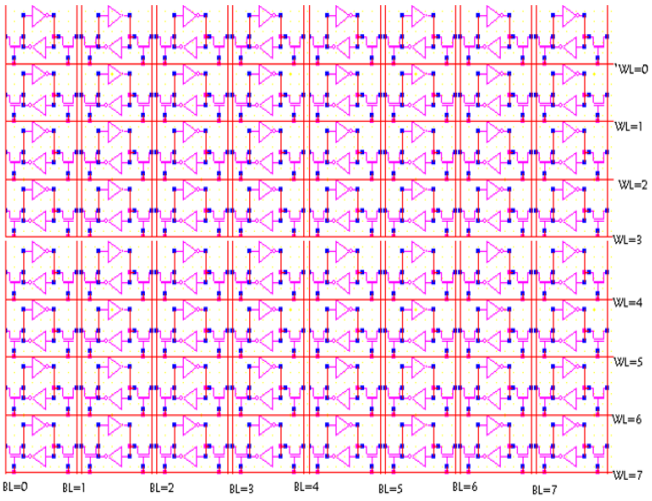

Figure 4: 64-BIT 6 T SRAM

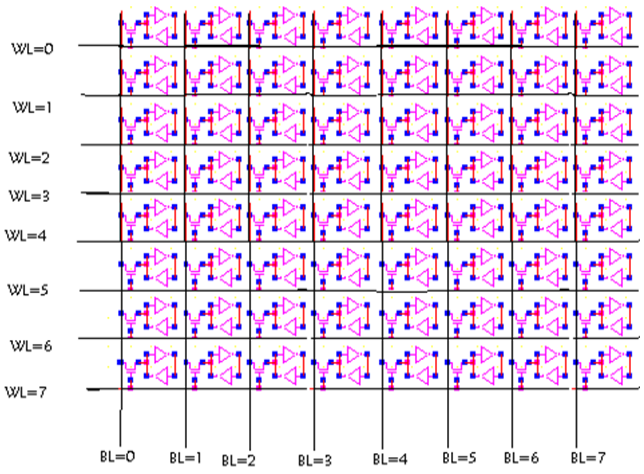

Figure 5: Block diagram of 5T 64-bit SRAM

Figure 5.4 is the 5T 64 bit SRAM structure. In this diagram 8 rows and 8 columns use in which 8 bit line and 8 word line use for operation.

To implement in 64bits 5T by using a 2.5µm technology gives the advantage of reduction of power dissipation in 37%, leakage current reduction is 36% and reduction of area is 30.16%.

II. LAYOUT DESIGN OF 1-BIT 5T SRAM BY USING 90N TECHNOLOGY

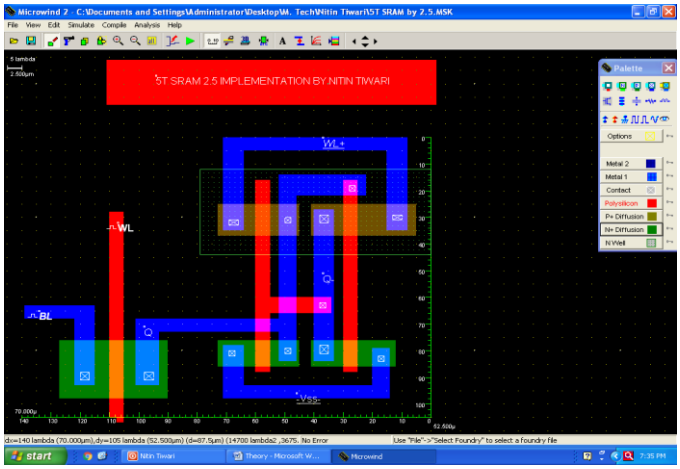

Figure 6: Layout Design of 1-Bit 5T SRAM by Using 2.5µm Technology

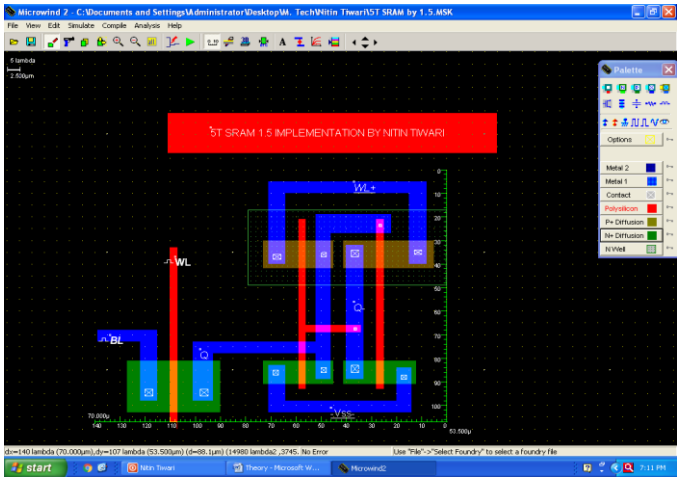

Figure 7: Layout Design of 1-Bit 5T SRAM by Using 1.5µm Technology

Table 1: Comparison between 1 Bit 6T and 5T SRAM

Performance Parameter	2.5µm 1.5µm 1-bit 6T SRAM		2.5µm 1.5µm 1-bit 5T SRAM	
Power Consumption	0.155 mW	0.207 mW	99.509µW 0.099mW	0.130mW
Layout Area	97.5*55 =5362.5 μm^2	97.5*55 =5362.5 μm^2	70*53.5 =3745 μm^2	70*53.5 =3745 μm^2
Diagonal of Layout	111.9 µm	111.9 µm	88.1 µm	88.1 µm
No of Transistor	6	6	5	5
Leakage Current	0.031mA	0.041mA	0.020mA	0.026mA

III. LAYOUT DESIGN OF 64-BIT 6T SRAM BY USING 2.5µM TECHNOLOGY

Figure shows Layout design of 64-bit 6T SRAM by using 2.5µm technology. The 64-bit SRAM is designed by using 1-bit

SRAM in which all 1-bit SRAM are arranged in row and column.

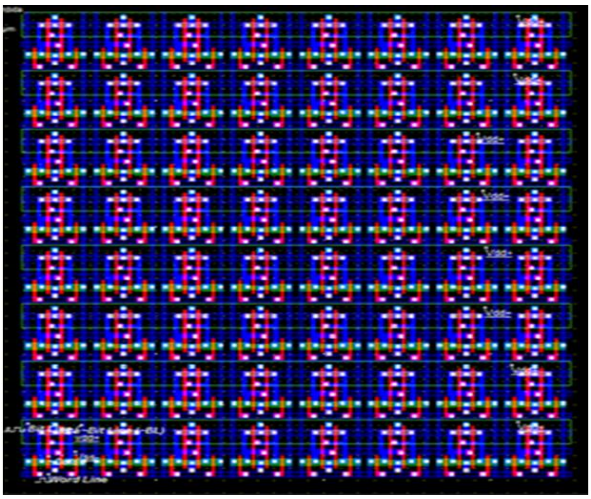

Figure 8: Layout Design of 64-BIT 6T SRAM by Using 2.5µm Technology by Microwind software

In this layout-

Power consumption = 0.155*64 mW = 9.92mW

Layout area = $(5362.5)\mu m^2$*64 =343200μm^2

No. of transistor = 6*64 = 384

Leakage currents $I_{dd\,(avr)} = 0.031 * 64 = 1.984mA$

IV. LAYOUT DESIGN OF 64-BIT 5T SRAM BY USING 2.5µM TECHNOLOGY

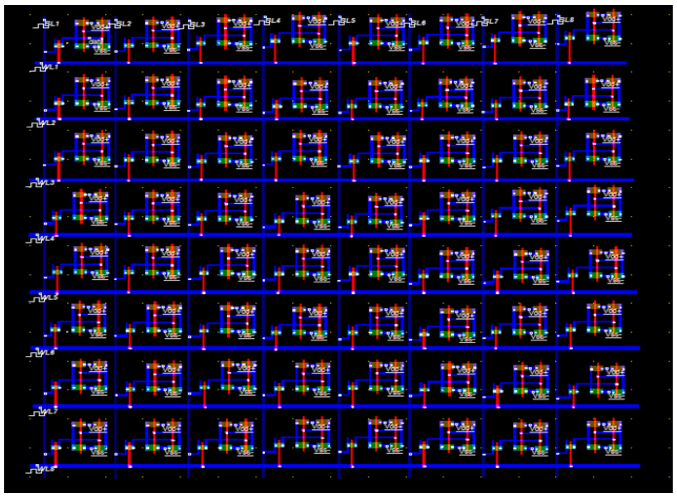

Figure 9: Layout Design of 64-BIT 5T SRAM by Using 2.5µm Technology by Microwind software

In this layout-

Power consumption is = 0.099*64 mW = 6.336mW

Layout area = $(3745)\mu m^2$*64 = 239680μm^2

No. of transistor = 5*64 = 320

Leakage currents $I_{dd\,(avr)} = 0.020 * 64 = 1.28mA$

Similarly follow the same technique for 1.5µm Technology and obtain the following results-

V. FOR LAYOUT OF 64-BIT 6T SRAM BY USING 2.5µM TECHNOLOGY-

Power consumption = 0.207*64 mW = 13.248mW

Layout area = $(5362.5)\mu m^2$*64 = 343200μm^2

No. of transistor = 6*64 = 384

Leakage currents $I_{dd\,(avr)} = 0.041 * 64 = 2.624mA$

VI. FOR LAYOUT OF 64-BIT 6T SRAM BY USING 1.5µM TECHNOLOGY-

Power consumption = 0.130*64 mW = 8.326mW

Layout area = $(3745)\mu m^2$*64 = 239680μm^2

No. of transistor = 5*64 = 320

Leakage currents $I_{dd\,(avr)} = 0.026 * 64 = 1.664mA$

CONCLUSION

A. Comparison between 64 BIT 6T and 5T SRAM

Table 2: Comparison between 64 BIT 6T and 5T SRAM

Performance Parameter	2.5µm 1-bit 6T SRAM	1.5µm	2.5µm 1.5µm 1-bit 5T SRAM	
Power consumption	9.92mW	13.248 m	6.336mW	8.326mW
Layout area	343200 μm^2	343200 μm^2	239680 μm^2	239680 μm^2
No. of transistors	384	384	320	320
Leakage currents	1.984mA	2.624mA	1.28mA	1.664mA

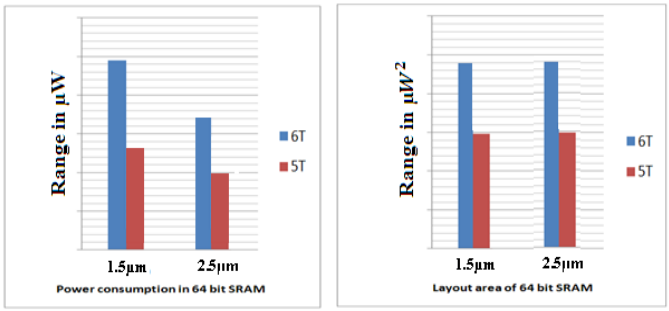

Figure 10: Comparisons between 64 Bit 6T and 5T SRAM

In this paper we conclude that we have implement 64 bit 5T SRAM which reduce 36.2% of power dissipation in 2.5µm and 37.2% in 1.5µm technologies over the 64 bit 6T SRAM. Also leakage current reduction in 5T SRAM over the 6T SRAM is $I_{dd\,(avr)}$=35% and $I_{dd\,(avr)}$=36.6% in 2.5µm and 1.5µm respectively. As well as area reduction in 5T SRAM over the 6T SRAM is 30.2% in both 2.5µm and 1.5µm.

References

[1] Kanika Kaur and Arti Noor," Strategies & Methodologies For Low Power Vlsi Designs: A Review", International Journal of Advances in Engineering & Technology, May 2011.

[2] B. Amelifard, F. Fallah, and M. Pedram, "Low-leakage SRAM design with dual Vt transistors", in Proc. of International Symposium on Quality of Electronic Design, 2006, pp. 729 -734.

[3] H.Mangalam and K.Gunavathi ," Gate And Subthreshold Leakage Reduced Sram Cells "Dsp Journal, Volume 6, Issue 1, September, 2006.

[4] G. Razavipour, A. Afzali-Kusha, and M. Pedram " Design and Analysis of Two Low Power SRAM Cell Structures "To appear in IEEE Transactions on VLSI Systems.

[5] Pushpa Saini and Rajesh Mehra," A Novel Technique for Glitch and Leakage Power Reduction in CMOS VLSI Circuits," International Journal of Advanced Computer Science and Applications, Vol. 3, No. 10, 2012.

[6] Eitan N. Shauly," CMOS Leakage and Power Reduction in Transistors and Circuits: Process and Layout Considerations", J. Low Power Electron. Appl. 2012, 2, 1-29; doi:10.3390/jlpea2010001.

[7] Valentino Crespi, Aram Galstyan and Kristina Lerman,"Comparative Analysis of Top–Down and Bottom–up Methodologies for Multi–Agent System Design,"AAMAS'05, July 2529, 2005, Utrecht, Netherlands.Copyright 2005 ACM 1595930949/05/0007.