Abstract—The Systematic Cell Design Methodology (SCDM) based on transmission gate in the category of hybrid-CMOS Logic style is proposed. All simulations have been performed with TSMC 0.125-μm technology, in an ideal state of the circuits to achieve the minimum power and delay. They also outperform their counterparts exhibiting reduction in power and reduction in delay. The simulation results demonstrate the delay, power consumption at different supply voltage.

Keywords—Systematic Cell Design Methodology, Three Input XOR/XNOR, Energy Efficiency, Binary Decision Diagram

I. INTRODUCTION

Building low-power VLSI system has emerged a significant performance goal because of the fast technology in mobile communication and computation. So the designers are faced with more constraint; high speed, high throughput and at the same time, consumption of power as minimal as possible.[3] The exclusive-OR (XOR) and exclusive-NOR (XNOR) gates are the essential parts of several digital systems and are highly used in very large scale integration (VLSI) systems such as parity checkers, comparators, crypto processors arithmetic and logic circuits, test pattern generators, especially in Full adder module as Sum output that is 3-input XOR and so forth. In most of these systems, XOR and XNOR gates constitute a part of the critical path of the system, which significantly affects the worst-case delay and the overall performance of the system.[4] A formal design method for balanced 3-input XOR–XNOR circuits in the hybrid-CMOS logic style. In our approach, we start with selecting a basic cell including 3-input and two outputs. Next and if necessary we apply various correction mechanisms and optimization methods to obtain balanced 3-input XOR–XNOR circuits. Accordingly and by using four basic cells, we come up with six balanced 3-input XOR–XNOR circuits. Full swing outputs impact multi-stage structured arithmetic circuit performance. Therefore, designers consider achieving full swing output operations as an important factor in the basic block design of arithmetic circuits. In addition, all of the proposed circuits whose critical path contains only two transistors have low average power consumption and delay [1]. As a consequence, most of them suffer from some different disadvantages [3]. They have voltage swing in some internal nodes due to logic style in which they are implemented, which leads to static power dissipation. 2. They suffer from severe output signal degradation and cannot withstand low-voltage operation. 3. They mostly have dynamic power consumption for non-balanced propagation delay inside and outside circuits, which cause glitches at the outputs. Design proposed in literature so far concentrate on creative design ideas but do not follow a systematic approach. SCDM (Systematic Cell Design Methodology), which is an extension of CDM, plays the essential role in designing efficient circuits. As an especial feature, the critical path of the presented designs consists of only two transistors, which causes low propagation delay, low VDD operations, low static power dissipation, avoids any degradation on the on the output voltage, increased the driving capability. After the systematic generation, the SCDM considers circuit optimization based on our target in three steps: 1) selection of the basic cell; 2) selection of the correct mechanisms; and 3) transistor sizing. It should be noted that Binary decision diagram can be utilized for Elementary basic cell generation of other three-input functions. The rest of this report is organized as follows. Section II Literature review on several papers. Section III presents comparison of advantages and disadvantages of different papers. The conclusion of this survey is given in Section IV.

II. LITERATURE REVIEW

The following section consists of systematic cell designs for energy and efficient to undergo the survey to obtain the better solution for low power operation of methodology.

A. Elementary Basic Cell

The methodology for three-input XOR/XNORs is presented according to the flowchart Fig.1. The design path is started by EBC systematic generation. In this step, general design goals are considered that the most distinctive ones are generating fairly balanced outputs, symmetric and power-ground-free structure, fewer transistors in the critical path, as well as sharing common sub circuit. In the remaining steps, the methodology offers opportunity to strive toward an assigned design target. Two of these steps include wisely selection of mechanisms and basic cells from PDP point of view. In order to generate the EBC of three-input XOR/XNOR circuits, four steps are taken. Initially, three-input XOR and its complement is represented by one binary decision tree (BDT) [8] in order to share common sub circuits. The BDT is achieved by some cascaded 2 ×1 MUX blocks. [10] which are denoted by simplified symbol controlled with input variables at each correspondent level. The step is followed by applying reduction rules to simplify the BDT representation. These include elimination, merging and coupling rules. The major task of the coupling rule, in simple terms, is to obtain all the possible equivalent trees by interchanging the order of the controls. Afterward, as the inputs into the first level are 0’s and 1’s of the function’s truth table, the 0 and 1 can be replaced by the Y and Y’, respectively.

Figure 1: Methodology for three-input XOR/XNORs
In the process of designing balanced 3-input XOR-XNOR circuits, we face three independent inputs and two...
complementary outputs. The result of applying the reduction rules and the substitution and disjoining to the trees.

**B. XOR-XNOR Circuits**

The proposed XOR and XNOR circuits are based on the modified version of a CMOS inverter and pass transistor logic. In proposed circuit-I, for XOR when the input B is at logic 1, the inverter circuit functions like a normal CMOS inverter. Therefore, the output is the complement of input A. When the input B is at logic 0, the CMOS inverter output is at high impedance. However, the ass transistor is ON and the output gets the same logic value as input A. The operation of the whole circuit is thus like a 2-input XOR circuit. However, it performs non full-swing operations for some input patterns causing their corresponding outputs to be degraded by |Vth|.

The proposed XOR-XNOR circuit-I is shown in Fig. 2. The output voltage levels of this circuit for each input combination .In proposed circuit-I when the input B is at logic 1, the PMOS pass transistor is OFF and NMOS pass transistor is ON. Therefore, the XOR output of the circuit is the complement of input A and XNOR output gets the same logic value as input A. When the input B is at logic 0, the XNOR output of the circuit is the complement of input A and XOR output gets the same logic value as input A for the reason that PMOS pass transistor is ON and NMOS pass transistor s OFF. The cross-coupled two PMOS transistors and two cross coupled PMOS and NMOS transistors are connected between XOR and XNOR outputs. This arrangement eliminates the non-swing operation.

Aspect ratio of the inverter circuit must be high for high driving capabilities.

![Figure 2: The XOR/XNOR circuit-I](image)

**C. Conventional Full Adder**

The conventional CMOS 28 transistor Full adder is considered as one of the Base case throughout this paper. The circuit is having inputs are a, b, cin and the sum, cout are the outputs of the one bit conventional 28 transistor full adder of 180 nm technology. The one bit full adder is implemented with 130 nm technology. In hybrid-CMOS[2] architecture, we get XOR and XNOR operations as module I. Module I circuit is an XOR - XNOR circuit. Many XOR-XNOR circuits are proposed by many authors. Circuit uses only 6 transistors and provides full output swing. This circuit is widely used in hybrid CMOS logic style. Module II and Module III are for the both sum and carry generation as individually. Here we have combined the three modules and designed the one bit full adder of 16 transistors for the 130 nm technology. The carry-select adder generally consists of two ripple carry adders and a multiplexer. In order to perform the calculation t recommendations. The addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application-specific digital signal processing (DSP) architectures and microprocessors. This module is the core of many arithmetic algorithms such as addition/subtraction, multiplication, division and address generation. The proposed circuit-I when the input B is at logic 1, the PMOS pass transistor is OFF and NMOS pass transistor is ON. Therefore, the XOR output of the circuit is the complement of input A and XNOR output gets the same logic value as input A. When the input B is at logic 0, the XNOR output of the circuit is the complement of input A and XOR output gets the same logic value as input A for the reason that PMOS pass transistor is ON and NMOS pass transistor s OFF. The cross-coupled two PMOS transistors and two cross coupled PMOS and NMOS transistors are connected between XOR and XNOR outputs. This arrangement eliminates the non-swing operation.

Aspect ratio of the inverter circuit must be high for high driving capabilities.

**Figure 2: The XOR/XNOR circuit-I**

As per the assumption of the carry being logic zero and the other assuming logic one. The above carry-select adder block size is 4. Two 4-bit ripple carry adders are multiplexed together, where the resulting carry and sum bits are selected by the carry-in. Since one ripple carry adder assumes a carry-in of 0, and the other assumes a carry-in of 1, selecting which adder had the correct assumption via the actual carry-in yields the desired result. The above application can be used anywhere at communication systems and portable electronic devices. The below figure 5 shows the 4-bit carry select adder layout for 130 nm technology.

**D. Alternative Logic Structure for Full Adder**

The Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application-specific digital signal processing (DSP) architectures and microprocessors. This module is the core of many arithmetic algorithms such as addition/subtraction, multiplication, division and address generation. As stated above, the PDP exhibited by the full-adder would affect the system’s overall performance. Thus, taking this fact into consideration, the design of a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital systems. Full adder is combinational circuits that form the arithmetic sum of three inputs bits. In full adder there is a three inputs and two outputs. In our block diagram we use three inputs as A, B, Ci. The third input is carry input. The outputs are SUM and CARRY. These full adder uses inverter based technologies, where not signals are generated internally control the functions of full adder. This helps to produce full voltage swing and no extra delay thus reducing overall propagation delay. Delay in full adder is nothing but amount of energy utilized in performing the determined task. The main parameters for designing a full adder is delay, power consumption, area and speed.

**Figure 3: Block diagram of 4-bit carry select Adder**

**E. Design Approach of Proposed Full Adder**

The full adder consists of 3 modules as shown in figure 1. Module 1 basically for implementation of XNOR circuit. Module 2 is for generation of SUM output using XNOR circuit whereas Module 3 is for carry generation Structure of
proposed full adder cell. Sum part of full adder is implemented using XNOR modules. The inverter comprises of transistors Mp1 and Mn1 will generate A’ which can be used to design the controlled inverter using Mp2 and Mn2.output of this inverter is XNOR of A and B. But because of the problem of voltage degradation Mp3 and Mn3 are introduced. Sum function implemented by second stage containing pmos transistors (Mp4, Mp5and Mp6) and nmos transistors (Mn4, Mn5 and Mn6). Similarly carry is implemented by using nmos transistors (Mn6 and Mn7).

The XNOR module is the main module of full adder. If the power consumption of the XNOR module is reduced then the full adder power consumption can be minimized. The modification in carry block makes the circuit work functionally different so that the power is reduced. The carry module is implemented by multiplying (A XOR B) with C and then multiplying (A XNOR B ) with the input A.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>(A XOR B)/C</th>
<th>(A XNOR B)/A</th>
<th>CARRY</th>
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<tr>
<td>0</td>
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### Table 1: Modified carry Table

III. COMPARISON OF LITERATURE REVIEW

<table>
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<th>REF NO</th>
<th>METHODOLOGY</th>
<th>PROS</th>
<th>CONS</th>
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<tr>
<td>[6]</td>
<td>Tree Structured Arithmetic Circuit</td>
<td>circuit is simple</td>
<td>Different full adder and cascaded adder circuit are implemented</td>
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<tr>
<td>[7]</td>
<td>Cell Design Methodology</td>
<td>Reverse converters that utilize the gate power</td>
<td>Expensive of eliminate the gate powers</td>
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<tr>
<td>[8]</td>
<td>Energy Recovery Theory</td>
<td>Power consumption</td>
<td>Produced by the low speed, low noise immunity</td>
</tr>
<tr>
<td>[9]</td>
<td>Fast Sign Detection Algorithm</td>
<td>Separate carry save adder comparator and carry generator unit are created</td>
<td>Single circuit is implemented</td>
</tr>
<tr>
<td>[10]</td>
<td>Power and Delay Comparison</td>
<td>CDM used to design efficient power circuit</td>
<td>Reduction area there by power dissipation</td>
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</table>

### CONCLUSION

In the end, new high performance three-input XOR/XNOR circuits with less power consumption and delay during SCDM. The new circuits enjoy higher driving capability, transistor density, noise immunity with low-voltage operation, and the least probability to produce glitches. As a unique feature, the critical path of the presented designs consists of only two transistors, which causes low propagation delay. On average, these circuits outperform their counterparts with 17%–53% reduction in power and 22%-77% reduction in delay respectively, in Tanner simulation based on the TSMC 0.125-μm technology. Simulation results show that the proposed circuits exhibit better performances compared to previously suggested circuits. Finally, we also classify the basic cells and the mechanisms based on performances and applications.

**References**


