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VLSI Implementation of Adder-less Multiplier: Line Multiplier

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Abstract— Line multiplier is a novel way of multiplication. In Digital signal processing operation multiplication is heavily used arithmetic operation and performance of processor depends on multiplier performance. So designing a low power multiplier is essential. In this paper line multiplier is implemented which is adder-less so easy to implement. Also no need to select or design an adder circuitry. In this paper line multiplier is designed and implemented on FPGA platform using Spartan 3 FPGA kit.

Keywords— *Multiplier, FPGA.*

I. INTRODUCTION

Multiplication is used in digital signal processor such as MAC, ALU and also microprocessor [1]. An important fundamental function in arithmetic logic operation in digital signal processor is a multiplier. Computational performance of a DSP system is limited by its multiplication performance [2].

Addition and multiplication operation dominates the execution time because statics shows that more than 70% instructions in microprocessor and most of DSP algorithms perform addition and multiplication [3] so there is demand of high speed multiplier is increasing to expand applications of computer and signal processing [3].

Multiplication is the process of adding a number of partial products. Multiplication algorithms differ in terms of partial product generation and partial product addition to produce the final result [4]. With time applications, many researchers have tried to design multipliers which offer either of the following- low power consumption, high speed, regularity of layout and hence less area or even grouping of them in multiplier. However, the two design criteria are often in conflict and that improving one particular aspect of the design constrains the other [4].

There are many number of multiplier which are array multiplier, booth multiplier, Wallace tree multiplier and vedic multiplier. With each have some advantages and disadvantages. This paper summarizes study of Line multipliers with Conventional multiplier. Section II explained Literature survey of multipliers. Section III explained basic working of Line multiplier. Results are described in Section IV. Finally conclusion of the paper is given in Section V.

Line multiplier is an adder-less multiplier so it requires less area, low power. Line multiplier multiplies two integers Numbers as follows: 1) selects lines according to multiplier and multiplicand.2) Switch matrix is used for calculating the multiplication.

II. LITERATURE SURVEY

In multiplication most basic form is consists of generation of the partial product of two binary numbers and partial product addition. Multiplication algorithms differ on the basis of way to partial product generation and partial product addition to produce the final result [4]. n number of partial products of m bit each is formed for (m*n)bit multiplication[5].

There are different types of Multipliers:

1. Array Multiplier
2. Booth Multiplier
3. Wallace multiplier
4. Vedic Multiplier

All the multipliers have their own advantages and disadvantages. There are some factor which decides the essential multiplier: Power- multiplier should consume Less power, Area- should have less slice and LUT's, Accuracy- should give correct result, Speed- should perform operation at high speed.

A. Array Multiplier

Array multiplier is one of the well know multiplier because of its regular structure it uses add-shift algorithm [8]. The partial product are shifted according to their bit sequences and then added. The summation can be performed with normal carry propagation adder. N-1 adders are required where N is the no. of multiplier bits [3].

B. Wallace Multiplier

In 1964, C.S.Wallace observed that it is possible to find a structure, which performs the addition operation parallel resulting in less delay [9].

C. Booth multiplier

Booth multiplier is another type of multiplier which reduces the number of partial products [5].The decision to use a Radix-4 modified Booth algorithm rather than Radix-2 Booth algorithm is that in Radix-4, the number of partial products is reduced to n/2. Though Wallace Tree structure multipliers could be used but in this format, the multiplier array becomes very large and requires large numbers of logic gates and interconnecting wires which makes the chip design large and slows down the operating speed [3].

D. Vedic Multiplier

Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in early twentieth century [6].

Vedic multiplier is the high speed multiplier it uses sutra to calculate the multiplication of numbers. Urdhva Tiryagbhyam and nikhilam are the two types of sutras.

In that Urdhva Tiryagbhyam vedic multiplier, Partial products are generated by concurrent addition of partial product [7] and the delay associated is mainly the time taken by the carry to propagate through the adders which form the multiplication array. So this is not an effective algorithm for multiplication of large numbers [2].

Another is the Nikhilam vedic multiplier which means "all from 9 and last from 10".when numbers involved is large then this multiplier is efficient i.e. less complex when large original numbers [1].

III. PROPOSED WORK

This proposed system is a novel way of multiplication which is Line Multiplier, which will calculate multiplication of two integer numbers by drawing line according to the numbers. The line multiplier is as shown below;

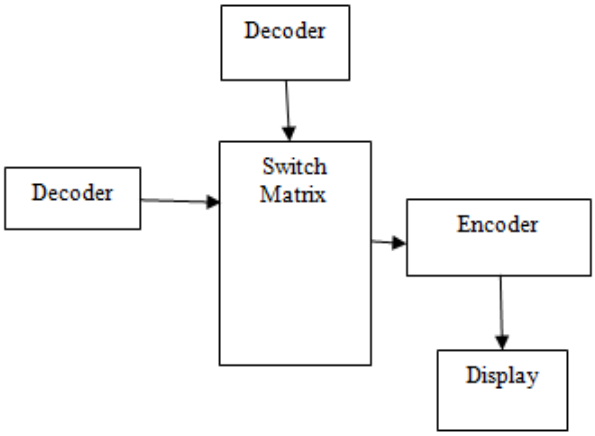

Figure 1: Line Multiplier

Fig. 1 shows block diagram of Line multiplier which is consist of Decoder, switch matrix, encoder and Display.

Decoder is a block which converts the given input of binary number into active line which is proportional to the given input. There are two decoders used for two operands separately. This is made up of logic gates.

Next block is switch matrix, consist of number of pass transistors. Switch matrix takes input from two decoders and produces output of multiplication. In this matrix only on pass transistor is active for one of the multiplication operation.

Another block is Encoder, encoder is converts one form of data into another type. Here encoder converts active line into BCD logic and this result is displayed on display.

A. Process to calculate multiplication

Fig. 2 shows how the line multiplier calculates the multiplication of number. In fig.2(a) two lines are drawn for multiplicand and then over these lines number of lines are drawn equal to multiplier as shown in fig. 2(b). Then count the number of intersection of lines as shown in fig. 2(c) and this is the result of multiplication.

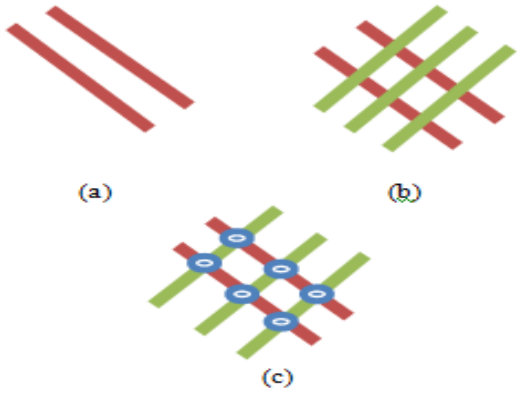

Fig. 2 Operation of line multiplication

No of intersection= Result of Multiplication of two integers

IV. RESULT

Line multiplier is implemented on Spartan-3 FPGA kit. Here fig. 3 shows 2*2 bit module of line multiplier and Fig. 4 shows design summary of multiplier.

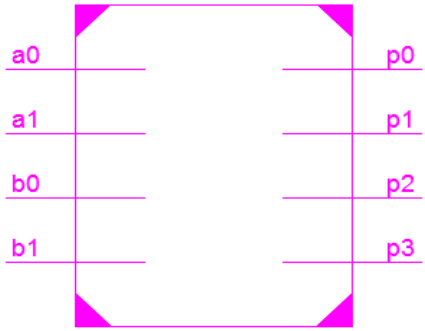

Figure 3: Line multiplier for 2*2 bit module

Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	13	1,920	1%
Total Number of 4 input LUTs	13	1,920	1%
Number of bonded IOBs	8	66	12%

Figure 4: Design summary of 2*2 bit line multiplier

Fig. 5 shows the module of 4-bit multiplier which has 16-number of bounded input outputs. Fig. 6 shows device utility of 4*4 bit multiplier.

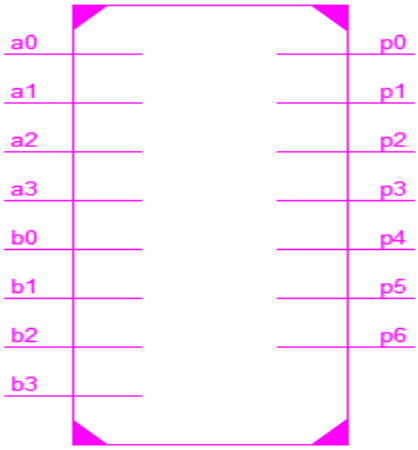

Figure 5: Line multiplier for 2*2 bit module

Device Utilization Summary			
Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	0	126,800	0%
Number of Slice LUTs	83	63,400	1%
Number of occupied Slices	33	15,850	1%
Number of bonded IOBs	15	210	7%

Figure 6: Design summary of 2*2 bit line multiplier

CONCLUSION

This paper presents a highly efficient method of multiplication. Authors implemented the code on Xilinx FPGA Spartan 3 board. The computational path delay for proposed 4*4 bit line multiplier is found to be 5ns. It is observed that the Line multiplier is much more efficient than Booth multiplier in terms of execution time (speed).

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