Comparative Analysis of Five Level Diode Clamped Multilevel Inverter with Spwm Control Strategy for Different Triangular Carrier Wave Configuration

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Abstract—The general function of the multilevel inverter is to synthesize a desired AC voltage from several levels of DC voltages. As the number of voltage levels increases the harmonic content decreases significantly. These multilevel inverters are used to increase inverter operating voltage, to minimize THD with low switching frequency, to reduce EMI due to lower voltage steps. Multilevel inverter technology has emerged recently as a very important alternative in the area of high power medium voltage energy control. This paper presents literature review on various multilevel converter PWM modulation strategies and simulation analysis of five-level diode-clamped multilevel inverter with one of its modulation strategy like SPWM with various triangular carrier wave configuration, which affect the %THD value and voltage level magnitude of the output voltage. The main objective of this study is to reduce total harmonic distortion, comparison of THD and fundamental component for different modulation techniques.

Keywords— Five level diode clamped multilevel inverter, SPWM technique, simulation analysis of MLI, Power converter.

I. INTRODUCTION

Inverter fed AC motor drives is the major application of power electronics circuits known as adjustable speed drives (ASD). PWM based inverters and multilevel inverters reduces the amplitudes of lower order harmonics in the terminal voltage by shifting the dominating harmonics towards higher frequencies.[1] Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. The term multilevel starts with the three-level inverter introduced by Nabaeet al. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage balance problems.

Three different topologies have been proposed for multilevel inverters[3]:-
1) Diode-clamped (neutral-clamped)
2) Capacitor-clamped (flying capacitors) and
3) Cascaded multilevel with separate dc sources.

But here we mainly discuss about Diode clamped multilevel inverter for five level and from various modulation strategies SPWM control strategy with various different triangular carrier wave configuration.

II. FIVE LEVEL DIODE CLAMPED MULTILEVEL INVERTER

According to patents the first multilevel inverter(MLI) was designed in 1975 and it was a cascade inverter with diodes blocking the source. This inverter was later derived into the Diode Clamped Multilevel Inverter(DCMLI), also called Neutral Point Clamped Inverter(NPC).[4] In this MLI the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Thus, the main concept of this inverter is to use diodes to limit the power devices voltage stress. Here Fig.1 presents one phase leg of the power circuit of a five-level NPCMLI.

For the power circuit of the Five Level NPCMLI shown in Fig. 1, the following useful relations is used. If ‘m’ is a number of level in output voltage waveform then the power circuit require (m-1) DC link capacitors, (m-1) (m-2) is the number of clamping diodes per phase, assuming that each blocking diode voltage rating is the same as the active device voltage rating and 2(m-1) is the number of switches with freewheeling diodes per phase. The maximum voltage stress on $V_{d}$ (m-1) the
switch is limited to the voltage across each capacitor which is equal to voltage across each capacitor. Output voltage (Van) waveform of Fig.1 is shown below with its switching sequence in Fig.2

Figure 1: One phase of the power circuit of a five-level NPCMLI

Figure 2a: Output Voltage (Van) Waveform for Five Level MLI

<table>
<thead>
<tr>
<th>OUTPUT VOLTAGE (Van)</th>
<th>Sa1</th>
<th>Sa2</th>
<th>Sa3</th>
<th>Sa4</th>
<th>Sa1’</th>
<th>Sa2’</th>
<th>Sa3’</th>
<th>Sa4’</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdc/2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Vdc/4</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>-Vdc/4</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>-Vdc/2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Figure 2b: Switching states of one Five level MLI Phase leg Where “1” means turned on and “0” means turned off

From switching states shown in Fig.2b half number of switches of a pole is always open for any voltage level and thus share the voltage stress equally, thus voltage rating of the switches is equal to voltage across one capacitor and the blocking voltage rating of the clamping diode is also equal to voltage across one capacitor. Here for the controlling purpose of this five level MLI, SPWM technique is used which is most popular now a days. In next section we discuss about various modulation strategies.

### III. CLASSIFICATION OF CONTROL STRATEGIES FOR MULTI LEVEL INVERTER

The main aim of the modulation strategy of multilevel inverters is to synthesize the output voltage as close as possible to the sinusoidal waveform. Many modulation techniques have been developed for harmonic reduction and switching loss minimization. The modulation methods used in multilevel inverters can be classified according to switching frequency[3], as shown in Fig.3

![Figure 3: Classification of Multilevel Modulation Methods.](image)

Methods that work with high switching frequencies have many commutation for the power semiconductors in one period of the fundamental output voltage. A very popular method in industrial applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage. Methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltages, generating a staircase waveform.

### IV. MULTILEVEL SINUSOIDAL PULSE WIDTH MODULATION (SPWM)

Instead of, maintaining the width of all pulses of same as in case of multiple pulse width modulation, the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the center of the same pulse. The distortion factor and lower order harmonics are reduced significantly. The control principle of the SPWM is to use several triangular carrier signals keeping only one modulating sinusoidal signal. For a m-level inverter, (m-1) triangular carriers are needed. The frequency of reference sinusoidal signal Fr determines the inverter output frequency and its peak amplitude A, controls the modulation index M, and rms output voltage Vo. The number of pulses per half cycle depends on carrier frequency. In SPWM Scheme, as shown in Fig.4, Gating signal is generated by high frequency triangular carrier wave(fc) compare with the low frequency (fr) sine wave.
Width of each pulse is varied in proportional to amplitude of sine wave.[11][8][5]

Phase opposition disposition (POD), where the carriers above the sinusoidal reference point are 180° out of phase with those below the zero point and this configuration is shown below in Fig.6

C. Alternative Phase Opposition Disposition (A POD) SPWM

Alternative phase opposition disposition (A POD), where each triangular carrier is phased shifted by 180° form its adjacent carrier as shown in Fig.7

D. Carrier Overlapping SPWM

Carrier overlapping SPWM, where each triangle carrier wave is overlapped by means of some percentage of value as shown below in Fig.8

E. Variable Frequency Carrier SPWM

For 5 level DCMLI from given four triangular carrier wave frequency of C1 and C4 is same but we can vary
the frequency of C2 and C3 up to the low or high frequency range. This type of configuration is as shown below in Fig. 9.

Figure 9: Waveform of Variable Frequency Carrier SPWM

V. SIMULATION ANALYSIS OF FIVE LEVEL DIODE CLAMPED MULTILEVEL INVERTER

A. Control circuit

Figure 10: Control Circuit of Diode Clamped MLI

B. Power Circuit

Figure 11: Simulation Model of Three Phase Diode Clamped MLI with RL Load

C. Waveforms

Figure 12: Waveforms of Pole Voltage, Line Voltage, Phase Voltage with Load Current

VI. SIMULATION RESULTS

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Modulation Index</th>
<th>Type of carrier wave arrangement</th>
<th>Pole voltage (Van)</th>
<th>Line voltage (Vab)</th>
<th>%THD of Van</th>
<th>%THD of Vab</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>0.7</td>
<td>Phase disposition (PD) SPWM</td>
<td>113.0 / 7</td>
<td>186.8 / 5</td>
<td>40.31 %</td>
<td>24.45 %</td>
</tr>
<tr>
<td></td>
<td>0.9</td>
<td></td>
<td>114.9 / 1</td>
<td>189.8 / 5</td>
<td>39.86 %</td>
<td>23.82 %</td>
</tr>
<tr>
<td></td>
<td>1.1</td>
<td></td>
<td>116.8 / 5</td>
<td>193.0 / 7</td>
<td>39.57 %</td>
<td>23.20 %</td>
</tr>
<tr>
<td></td>
<td>1.3</td>
<td></td>
<td>118.5 / 1</td>
<td>195.8 / 6</td>
<td>39.12 %</td>
<td>22.58 %</td>
</tr>
<tr>
<td>2.</td>
<td>0.7</td>
<td>Alternative phase opposition (APOD) SPWM</td>
<td>113.1 / 1</td>
<td>189.6 / 4</td>
<td>40.56 %</td>
<td>30.25 %</td>
</tr>
<tr>
<td></td>
<td>0.9</td>
<td></td>
<td>114.9 / 5</td>
<td>192.9 / 7</td>
<td>40.10 %</td>
<td>30.19 %</td>
</tr>
<tr>
<td></td>
<td>1.1</td>
<td></td>
<td>116.8 / 9</td>
<td>196.6 / 2</td>
<td>39.80 %</td>
<td>30.34 %</td>
</tr>
<tr>
<td></td>
<td>1.3</td>
<td></td>
<td>118.5 / 4</td>
<td>199.5 / 4</td>
<td>39.34 %</td>
<td>30.04 %</td>
</tr>
<tr>
<td>3.</td>
<td>0.7</td>
<td>Phase</td>
<td>113.2</td>
<td>193.2</td>
<td>40.11 %</td>
<td>36.22 %</td>
</tr>
</tbody>
</table>
CONCLUSION

This paper has provided a brief summary of multilevel inverter circuit topologies, their control strategies with mainly Sinusoidal Pulse Width Modulation (SPWM) with various configuration of triangular carrier wave as discussed earlier. By applying SPWM modulation techniques with various carrier wave configuration to Five level Diode Clamped multilevel inverters under consideration in simulation and from the simulation results as the modulation index is more than the value of rms pole and line voltages are more as well as the value of %THD also decrease significantly. And from all the technique of SPWM, Carrier Overlapping is good because from this technique we get more rms output line voltages and %THD of line voltage is also very less nearly 21.16% for modulation index 1.3 as compared to other technique for same switching frequency of carrier. So from simulation we can conclude that from above all discussed technique of SPWM ‘Carrier Overlapping SPWM’ control strategy is best for the Five level Diode Clamped MLI which is also used for industrial and other purpose’s.

References


3) Bindeshwar Singh, Nupur Mittal, Dr. Deependra Singh and Dr. K. S. Verma, “Multilevel Inverter: A Literature Survey on Topologies and Control Strategies,” IJIR, VOL.10, July 2012


