

A Study Between Intel 8085 and Intel 8086

Shreeanant Bharadwaj

Student, Department of Electrical and Electronics Engineering, Maharaja Agrasen Institute of Technology, Delhi, India

Abstract—In the following paper, we shall see features of the 8085 microprocessor and 8086 microprocessor and we will compare them briefly and will see which is better suited for the overall task.

Keywords—8085-Microprocessor, 8086-Microprocessor, Microprocessors, Microcontrollers

I. INTRODUCTION

A microprocessor is a controlling unit of a micro-computer, fabricated on a small chip capable of performing ALU (Arithmetic Logical Unit) operations and communicating with the other devices connected to it that are used by a computer to do its work. It is a central processing unit on a single integrated chip containing millions of very small components including transistors (The transistors are mostly MOSFETs), registers, and diodes that work together. Some microprocessors in the 20th century required several chips. Microprocessors help to do everything from executing the most basic daily tasks up to the very complex ones. Everything a computer does is described by a set of instructions, and microprocessors carry out these instructions many millions of times a second. Microprocessors were invented in the 1970s for use in embedded systems. The majority are still used that way, in such things as phones, automation, home appliances.

II. 8085 MICROPROCESSOR

A. 8085 Microprocessor

8085 microprocessor was designed by Intel in March 1976. It is an 8-bit software, binary compatible microprocessor. There are three types of buses in 8085 microprocessor Address bus, Databus, and Control bus. Address bus recognizes the data in memory, find or tells the location of data in 8085 microprocessor it is of 16 bits, Address bus has 16 bits that means 2¹⁶ bytes can be handled by 8085 microprocessor. Data bus carries data from memory, once the address or location is known, Data is being transferred. The control bus has two tasks either to read or to write on the location. 8085 is an 8-bit microprocessor as its ALU is of 8-bit size [1]. PC (Program Counter), is used for sequencing of programs, that is which instruction has to be executed after which one, that is controlled by PC, in simple words address of the next instruction is stored by PC [2]. The increment and decrement of PC are done by INC/DEC (Increment/Decrement) register [3]. The size of INC/DEC registers is 16 bits, as they work on PC, which stores an address of 16 bits [4]. Address buffer is a storage technique used by PC to store instruction's address here there are two address buffers, each of size 8 bit. One of the two buffers is used to store just address lines from 8 to 15 are A₁₅ to A₈, while the other line 0 to 7 are AD₀ to AD₇, these lines are multiplexed address and data bus. Data stored in the address buffer goes to the internal data Bus by a channel to IR (Instruction Register) [5]. Data fetched from memory is to be stored by IR. It only holds the data that is being fetched from the memory After IR comes ID which information decoder, It converts Data into 0s and 1s after it decodes comes the Timing and Control unit [6]. The timing and Control unit is like a brain to the microprocessor 8085 it provides information and control

signal to all the registers of the microprocessor. After T and C unit comes to ALU (Arithmetic Logical Unit), It is an 8-bit unit. B, C, A, E, H, and L are all 8 bit registers known as General purpose registers these registers are programmer-friendly because they can be programmed easily [7]. Register A or the Accumulator is not a programmer-friendly register, It always contains the first operand [7]. The second Operand is contained by the temporary (TEMP) register which stores the operand's value temporarily by taking the actual value from general-purpose registers which are given by the programmer [8]. The accumulator not only stores the first operand but also the output of the processor [9]. ALU receives two inputs from Accumulator and Temporary register and gives the result back to the accumulator through an 8-bit internal Data Bus. Flag Flip Flop does not contain output but the status of the output, they are known as status registers, SP is stack pointer it denotes the last elements stored in the stack that will be executed (because of the LIFO-Last In First Out concept). It also holds the address of the data (not the data but its address which is of 16 bit, that's why stack pointer has the size of 16 bit) [10]. During this whole process if any interrupt arises that is handled by the Interrupt controller, it works on two pins INTA (Interrupt acknowledged) and INTR (Interrupt Request). Serial I/O controller also works on two pins SID (Serial Input Data) and SOD (Serial Output Data). Programmers sometimes combine general-purpose registers to store 16 bits of data.

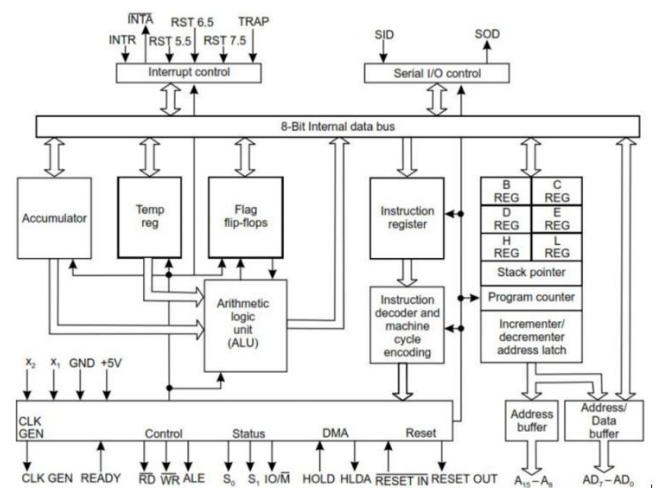


Figure 1: 8085 Architecture

B. Storage and Interface Unit of 8085

B, C, D, E, H, and L registers, are 8 bits registers that can be combined to form 16 bit registers, and that are BC, DE, and HL [11]. The program counter is utilized to point next instruction to get executed at a particular location and it leads to address line and data line [address latch-A₈ to A₁₅, address and data latch-AD₀ to AD₇].

C. Instruction Unit of 8085 Microprocessor

IR has data of the next instruction to get executed. ID decodes the instruction and after decoding it is given to the timing and control unit, where there are control signals. X₁ and X₂ are

interfaced crystal clock synchronized and calibrated with an 8085 microprocessor.

III. PIN DIAGRAM OF 8085

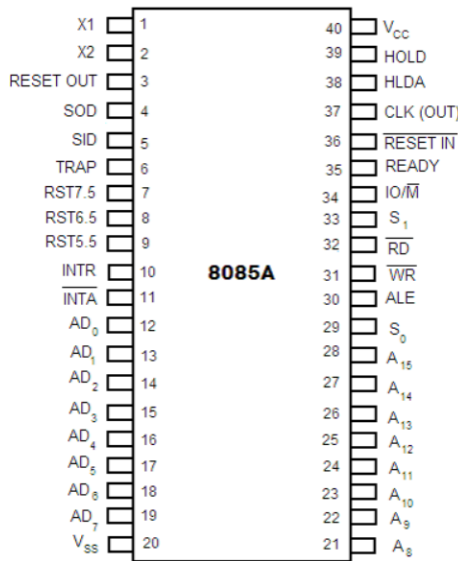


Figure2: 8085 Pin Diagram

```

1   LDA 2050
2   MOV H
3   LDA 2051
4   ADD H
5   MOV L,A
6   MVI A 00
7   ADC A
8   MOV H ,A
9   SHLD 3050
10  HLT
    
```

Figure 3: Program to add two 8 bit numbers in 8085 microprocessor

Pin 1 and 2 or X1 and X2 respectively are crystal clocks or frequency pins they maintain the internal frequency of 8085 microprocessor. Pin-3 or RESET OUT is reset output pin which resets the output as well as memory and I/O devices. Pin 4 and 5 are SID. SID is Serial Input Data and I/O devices transfer data, bit by bit serially through this pin. SOD is Serial Output Devices pin microprocessor gives data, bit by bit serially through this pin. Pin 6 to Pin 11 are Interrupt pins they manage Interrupts. There are two types of interrupts maskable interrupts and unmaskable interrupts. And the pins in priority order are TRAP, RST 7.5, RST 6.5, RST 5.5, INTR. Pin 12 to Pin 19 These are Address-Data multiplexed Bus, address bus are uni-directional and address-data bus are bi-directional, contains data and is used for transfer of data. Pin-20 or GND is the ground pin used for grounding. Pin 21 to Pin 28 are Address line pins (A8 to A15). Pin 30 -is ALE address latch enabled - it latches the address. Pin 29 to Pin 34 (except pin 30) are as following S0 and S1 are Status pins, IO/M are Input data memory bar, RD and WR are read and write pins respectively[12].

IO/M	S0	S1	Status
0	0	0	HALT
0	0	1	M-WRITE
0	1	0	M-READ
1	0	1	I/O-WRITE
1	1	0	I/O-READ
0	1	1	Opcode Fetch
1	1	1	INT-A

Pin-35 -READY -works when every pin of 8085 is in its position and then it is executed. Pin-36 **RESET** - \overline{IN} (resets input and by that it means I/O devices and the memory). Pin-37 CLK(OUT) keeps the record of the data in terms of time. Pin 38 and Pin 39 are HOLD and HLDA respectively they hold request and they acknowledge the requests respectively. Pin-40 is Vcc pin it provides +5V power supply[13].

IV. FEATURES OF 8086

8086 is a microchip designed by Intel between early 1976 and June 8, 1978. Intel 8086 Microprocessor has two units BIU (Bus Interface Unit) and EU (Execution Unit), It was the world's first 16-bit microprocessor, It supports pipelining, All microprocessors have three basic tasks to do Fetching, Decoding, and Execution. BIU is connected directly to memory with I/O (Input-Output) devices, there is no connection of EU and memory directly, the communication of EU with memory and I/O devices happens through BIU[14]. First data comes from memory or I/O devices to BIU and then from BIU it goes

to EU, where it is executed and the result will go back to BIU and then to I/O devices or memory[15]. The segment is a part of memory, for instance, 8086 has two Bus lines Data line and an Address line, Data line is 16 bits and the Address line is 20 bits. Since the size of the address line is 20 bits, so it can handle up to 2^{20} bytes of memory (2^{20} bytes is almost equal to 1 MB (Megabyte))[16]. CS (Code Segment) register, DS (Data Segment) register, SS (Stack Segment) register, ES (Extra Segment) register, IP (Input Pointer) register are not memory segments but are segment registers[17]. Segment registers are registers that contain the address of the segment, That is they store their respective segment's address location, as they store address so they should have the same size as the ALU (Arithmetic Logical Unit) of 8086 microprocessor which is 16 bit[17]. There are two types of addresses Virtual address and Physical address. The virtual address is the address that is user or programmer-friendly, while the physical address is machine-friendly it is in binary form.

There is another type of address that is calculated with the physical address and that is the Offset address[18]. A physical address can be easily calculated by the formula :

$$PA = SA * 10H + OA.$$

where PA is the physical address, SA is the segment address, 10H is 10 in hexadecimal system, and OA is the offset address. The physical address is given by segment registers and then the information moves to IQ (Instruction Queue) which has the size of 6 bytes (6 * 8 bits), IQ is responsible for the fast execution of 8086. After IQ information is transferred to the Control section of the architecture, which is referred to as the brain of the EU. In 8086 microprocessors, the general-purpose registers are divided into separate 8-bit parts so that if we want to store data that is 8 bits or less there is no point in wasting a

Table 1: Truth Table of IO/M, S0 and S1

16-bit register.SP is the Stack Pointer, It points at the Top of memory, BP is the Base pointer it points at the base of the memory.SI and DI are Source Index and Destination Index respectively.SI acts as the offset to DS and DI acts as the offset of ES.After this comes ALU, it takes two inputs and gives output based on the instruction given to it and the way it is programmed. The output of ALU is connected to the Flag register and the Temp(temporary) register.Flag register shows or calculates the status of the output, Flag has many registers in it but some common ones are zero registers,parity register, sign register, and size register. Ax(AH + AL),Bx(BH+BL),Cx(CH+CL),Dx(DH+DL),SP,BP,SI,DI all these are general-purpose registers,all of these registers are programmer friendly[19].

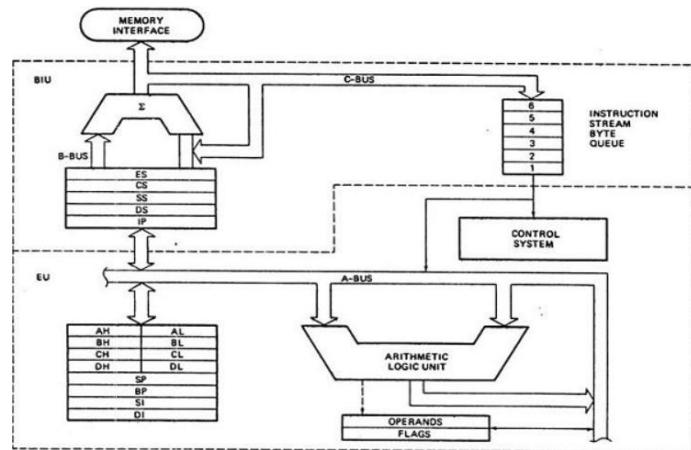


Figure 4: 8086 Architecture

```

1  MOV AL, [500]
2  MOV BL, [501]
3  ADD AL, BL
4  DAA
5  MOV [600]
6  MOV AL, 00
7  ADC AL, AL
8  MOV [601], AL
    
```

Figure 5: Program to add two 8 bit numbers in 8086 microprocessor

V. PIN DIAGRAM OF 8086

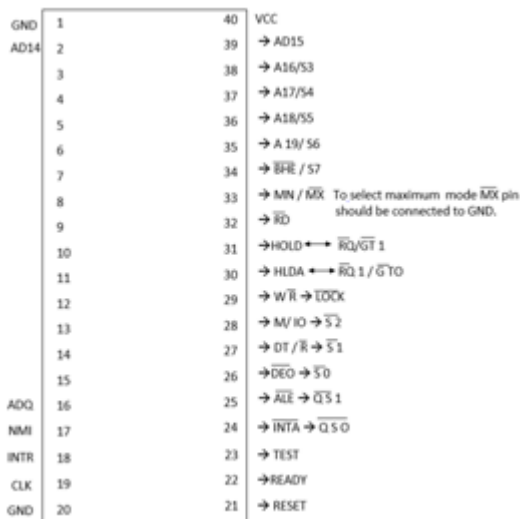
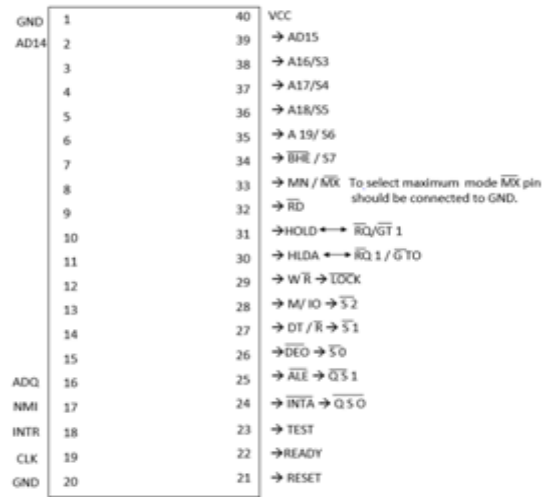


Figure 6: Pin Diagram of 8086



In microprocessor 8086 Pin 1 to Pin 23 and Pin 32 to Pin 40 are known as common pins as they work both in MAX mode and MIN mode. While the other pins from 24 to 31 are Non common pins as they work differently on different modes.

A. Common mode pins

Pin-1 is the GND pin which is the ground pin, it moves excessive electricity into the ground.Pin-2 to Pin-16 are AD14 to AD0, these pins are multiplexed addresses and data lines.Pin-17 is the NMI pin it is the non-maskable interrupt pin, it handles the interrupt that is not under the programmer's control.Pin-18 is an INTR pin it is the Interrupt Request pin, which requests the maskable interrupts. and can be programmed.Pin 19 is the CLK pin it is the Clock pin, all internal parts of the 8086 microprocessor are synchronized by this pin.Pin 20 is another GND pin.Pin 21 is the RESET pin, and as the name suggests it resets the whole architecture.Pin 22 is the READY pin, it tells whether external devices are ready to fetch data or not.Pin 23 is the TEST it works on WAIT instruction, if the processor is in WAIT state, then this pin works.Pin 32 is the RD pin, it is an active low pin.Pin 33 is MN/MX pin, If VCC is connected with this pin then MIN mode is enabled. If the GND pin is connected with this pin then MAX mode is enabled.Pin 34 is the BHE/S7 it Is the Bus high enabled pin.

Table 2: Truth Table of BHE and S7

BHE	S7	Operation
0	0	Whole (W)
0	1	Upper (ODD)
1	0	Lower (EVEN)
1	1	Idle state

Pin 35 is the A19/S6, this is the only pin that is reserved for future purposes, it has been set to default logic-0.Pin 36 is A18/S5 pin, it contains the value of the interrupt flag, which tells the status of the interrupt.Pin 37 and Pin 48 are A16/S3 and A17/S4, these pins tell the status, also tells which segment is being used.

Table 3: Truth table of A16/S3 and A17/S4

A16/S3	A17/S4	Segment
0	0	ES (Extra Segment)
0	1	SS (Stack Segment)
1	0	CS (Code Segment)
1	1	DS (Data Segment)

Pin 39 is AD15 it is another multiplexed address and data line. Pin 40 is a VCC pin it gives a +5 volt power supply to the processor.

B. Un-Common pins(MAX mode)

Pin 24 and Pin 25 are QS0 and QS1.

Table 4: Truth Table of QS0 and QS1

QS0	QS1	Operation
0	0	No Operation
0	1	First Byte from queue
1	0	Empty the queue
1	1	Subsequent byte from the queue

Pin 26 to Pin 28 are all active low signals.

Table 4: Truth table of $\overline{S0}, \overline{S1}$ and $\overline{S2}$

$\overline{S0}$	$\overline{S1}$	$\overline{S2}$	Operation
0	0	0	INTA
0	0	1	R I/O
0	1	0	W I/O
0	1	1	HALT
1	0	0	R Memory
1	1	0	W Memory
1	1	1	Idle state

Pin 29 is the LOCK pin it is used when the microprocessor is executing instruction from a resource, the resource is locked so that the process is not interrupted by other processors. Pin 30 and Pin 31 are $\overline{RQ/GT0}$ and $\overline{RQ/GT1}$ these are requested grant pins, these are important pins as when multiprocessors are connected with I/O devices and memory then, these pins request permission, and the main processor grants it.

C. Un-Common pins(MIN mode)

Pin 24 is the INTA pin, which is Interrupt acknowledgment pin. Pin 25 is the ALE pin which is an address latch enabled pin, this pin decides whether the Address line will be used or the data line will be used in multiplexed address and data line. If ALE is logic-0 then the address line is enabled, If ALE is logic-1 then the Data line is enabled. Pin 26 is the DEN pin, which is the Data-Enabled pin, if a data buffer is present in any data bus, then DEN is enabled or disabled to access that data buffer. Pin 27 is the DTR pin, it is Data transmit request pin. If DTR is logic 0 then the microprocessor transmits the data, If DTR is logic-1 then the microprocessor receives the data. Pin 28 is the $\overline{M/\overline{IO}}$, Microprocessor can either take data from memory or I/O devices, this pin tells whether data is being taken from Memory or I/O devices. Pin 29 is the WR pin which is the write pin. Pin 30 and Pin 31 are HOLD pin and HLDA pin respectively, these are Hold and Hold acknowledge pins. HOLD holds memory while accessing and HLDA acknowledges it.

VI. MAJOR DIFFERENCES BETWEEN 8085 AND 8086

Table 5: Comparison between features of 8085 and 8086

Measure	8085 microprocessor	8086 microprocessor
Data Bus Size	It is an 8-bit microprocessor	It is a 16-bit microprocessor
Address Bus	It has a 16-bit address bus	It has a 20-bit address bus
Memory	Can access upto 64 kb	Can access upto 1 Mb
Instructions	It does not have an instruction queue	It has an instruction queue
Pipelining	Does not supports pipeline architecture	Does support pipeline architecture
I/O Devices	Can address up to $2^8 = 256$ I/O devices	Can address up to $2^{16} = 65,536$ I/O devices
Cost	Cost is very less	Cost is very high
Multi-processor support	Does not supports multi-processing	It supports multi-processing
Arithmetic Support	Only supports integer and decimal	Supports integers, decimals, and ASCII character
Multiplication and Division	Does not supports multiplication and division	8086 microprocessor supports multiplication and division
Operating Modes	Supports only one mode	Supports two modes - MAX mode and MIN mode
Memory Segmentation	Memory space is not segmented	Memory space is segmented
Number of Processors	Only one processor is used	More than one processor is used. Additional processor (external) can also be employed
Clock Speed	3MHz	Varies in range 5.8 – 10 MHz
Flags	It has 5 flags (Sign, Zero, Auxiliary Carry, Parity, Carry)	It has 9 flags (Overflow, Direction, Interrupt. Trap, Sign, Zero, Auxiliary Carry, Parity, Carry)
Processor type	Accumulator based	General Purpose register based
Memory Size	64KB	1 MB
Number of transistors	Nearly 6500	Nearly 29000
Duty Cycle for clock	50%	33%

CONCLUSION

The 8085 is an 8-bit microprocessor. It was produced by Intel and first introduced in 1976. The 8086 is an enhanced version of the 8085 microprocessor. It is a 16-bit processor. Even though both are made at different times and intended for different purposes. The biggest advantage is address bus in 8086 is 20 bits and the data bus is 16 bits in a single clock cycle can operate 2 bytes word. So it gives much faster and better performance than 8085. 8086 data pins are of 16 bits, so execution time is unaffected for the 16-bit opcode to be read or write into memory locations, 8085 has 8-bit data pins thus it requires additional four clock cycles to fetch the 16-bit opcode. The 8086 has a 20-bit address bus, so it can address 2^{20} addresses. Each address represents a stored byte. To make it possible to read or write a word with one machine cycle, the memory for an 8086 is set up in 2 banks, i.e. Lower Bank and Upper Bank. The Upper Memory bank contains all bytes which have odd addresses while the Lower contains bytes of even addresses, if we read a byte from or write a byte to an even address the A0 will be low BHE will be high enabling the lower bank and disabling the upper bank. BHE stands for Bus High Enable, BHE is absent in 8085 and there is no such concept of banking. A0 and BHE signals prevent the writing of an unwanted signal. While entering HALT in minimum mode ALE is not delayed in 8086 but the ALE gets delayed by one clock cycle in 8085. So, yes there is enough difference in programming 8085 and 8086.

References

- [1] Mathur, Sunil, "Microprocessor 8085 and its interfacing", 2011, PHI Learning Pvt. Ltd., mathur2011microprocessor
- [2] Checkoway, Stephen and Davi, Lucas and Dmitrienko, Alexandra and Sadeghi, Ahmad-Reza and Shacham, Hovav and Winandy, Marcel, "Return-Oriented Programming without Returns" in Proceedings of the 17th ACM Conference on Computer and Communications Security 2010, pp 559-572, DOI: 10.1145/1866307.1866370
- [3] Lomont, Chris, "Introduction to x64 assembly" in Recuperado de: <https://software.intel.com/en-us/articles/introduction-to-x64-assembly> Programaci(\o)n en Python Referencias ,2012, lomont2012introduction
- [4] O. Cret, K. Pusztai, C. Vancea and B. Szente, "CREC: a novel reconfigurable computing design methodology," Proceedings International Parallel and Distributed Processing Symposium, 2003, pp. 8 pp.-, DOI: 10.1109/IPDPS.2003.1213323.
- [5] Smith, James E, and Dermer, GE and Vanderwarn, BD and Klinger, SD and Rozewski, CM, "The ZS-1 central processor" in ACM SIGARCH Computer Architecture News Press 1987, vol. 15, no. 5, pp 199-204, DOI: 10.1145/36206.36203
- [6] Flynn, Michael J, and others, "Computer architecture: Pipelined and parallel processor design", 1995, Jones & Bartlett Learning, flynn1995computer
- [7] Srinath, NK, "8085 Microprocessor: Programming and Interfacing", 2005, PHI Learning Pvt. Ltd., srinath20058085
- [8] Heath, Steve, "Embedded systems design", 2002, Elsevier, heath2002embedded
- [9] O. Cret, K. Pusztai, C. Vancea and B. Szente, "CREC: a novel reconfigurable computing design methodology," Proceedings International Parallel and Distributed Processing Symposium, 2003, pp. 8 pp.-, DOI: 10.1109/IPDPS.2003.1213323.
- [10] P. P. Silvester, "Introducing computer structure by machine simulation," in IEEE Transactions on Education, vol. 33, no. 4, pp. 326-332, Nov. 1990, DOI: 10.1109/13.61084.
- [11] K. M. Dostert, "Frequency-hopping spread-spectrum modulation for digital communications over electrical power lines," in IEEE Journal on Selected Areas in Communications, vol. 8, no. 4, pp. 700-710, May 1990, DOI: 10.1109/49.54466.
- [12] Mahalakshmi, "8051 Microcontroller Architecture, Programming and Application", 2012, Laxmi Publications, mahalakshmi20128051
- [13] R. Patel, W. Wong, J. Lam, T. Lai, T. White, and S. Cheung, "A 3.3-V programmable logic device that addresses low power supply and interface trends," Proceedings of CICC 97 - Custom Integrated Circuits Conference, 1997, pp. 539-542, DOI: 10.1109/CICC.1997.606684.
- [14] Johnsson, L, and Seitz, CL, "Submicron Systems Architecture", 1982, CALIFORNIA INST OF TECH PASADENA DEPT OF COMPUTER SCIENCE, johnsson1982submicron
- [15] Ortega, Tames M and Voigt, Robert G, "slam", ortegaslam
- [16] Brey, Barry B, "The Intel microprocessors: 8086/8088, 80186/80188, 80286, 80386, 80486, Pentium, Pentium Pro processor, Pentium II, Pentium III, Pentium 4, and Core2 with 64-bit extensions: architecture, programming, and interfacing", 2009, Pearson Education India, brey2009intel
- [17] Guide, Part, "Intel\{textregistered} 64 and ia-32 architectures software developer's manual" in Volume 3B: System programming Guide, 2011, Part, vol. 2, no. 11, guide2011intel
- [18] M. Gschwind, D. Erb, S. Manning, and M. Nutter, "An Open Source Environment for Cell Broadband Engine System Software," in Computer, vol. 40, no. 6, pp. 37-47, June 2007, DOI: 10.1109/MC.2007.192.
- [19] Jablin, Thomas B and Jablin, James A and Prabhu, Prakash and Liu, Feng and August, David I, "Dynamically managed data for CPU-GPU architectures" in Proceedings of the Tenth International Symposium on Code Generation and Optimization, 2012, pp 165-174, jablin2012dynamically
- [20] Chakraverty, Shampa, and Chakraborty, Pinaki and others, "A Peer-Assessment Based Approach for Teaching Microprogramming" in Journal of Engineering Education Transformations, 2021, Volume 34, Number 4, pp 12-17, DOI: 10.16920/jeet/2021/v34i4/146148
- [21] V.K. Jain and H.M. Gupta and S.N. Gupta, "Intel 8085 Microprocessor—A Tutorial Review" in IETE Technical Review 1984, Taylor & Francis, vol. 1, no. 12, pp 173-178, DOI: 10.1080/02564602.1984.11437661
- [22] Morse, Stephen P, and Pohlman, William B, and Ravenel, Bruce W, "The Intel 8086 Microprocessor: a 16-bit Evolution of the 8080", 1978, IEEE, vol. 11, no. 6, pp 18-27, morse1978intel
- [23] S. Morse, S. Mazor, W. Pohiman and B. Raveiel, "Intel Microprocessors?8008 to 8086" in Computer, vol. 13, no. 10, pp. 42-60, 1980.
- [24] Liu, Yu-Cheng and Gibson, Glenn A, "Microcomputer systems: The 8086/8088 family: Architecture, programming, and design", 2000, Prentice-Hall, Inc., liu2000microcomputer
- [25] Fukuda, Hiroaki, and Leger, Paul and Figueroa, Ismael, "A Practical Methodology to Learn Computer Architecture, Assembly Language, and Operating System" in CSEDU (1), 2020, pp 333-340, fukuda2020practical
- [26] Zhang, Ye, and Meina, A and Lin, Xuhao and Zhang, Kun and Xu, Zhen, "Digital Twin in Computational Design and Robotic Construction of Wooden Architecture" in Advances in Civil Engineering, 2021 vol. 2021, Hindawi, zhang2021digital
- [27] Srinath and NK, 8085 Microprocessor: Programming and Interfacing, 2005, PHI Learning Pvt. Ltd., srinath20058085,
- [28] Kant Krishna, "Microprocessors and Microcontrollers: Architecture, Programming and System Design 8085, 8086, 8051, 8096", 2007, PHI Learning Pvt. Ltd., kant2007microprocessors
- [29] Liu, Yu-Cheng and Gibson, Glenn A., "Microcomputer Systems: The 8086/8088 Family: Architecture, Programming, and Design", 2000, Prentice-Hall, Inc., USA, 10.5555/3701